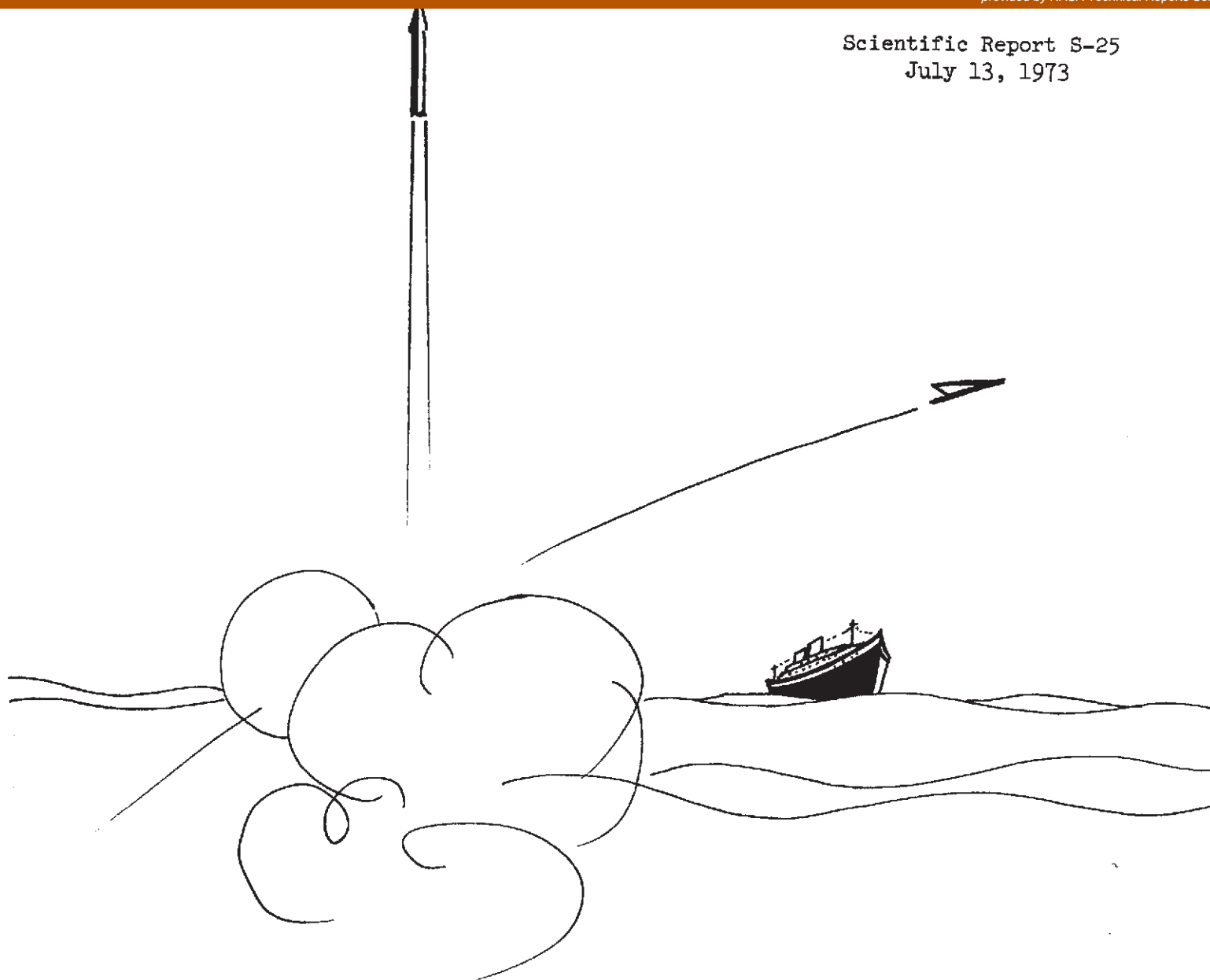


Scientific Report S-25
July 13, 1973



(NASA-CR-128333) DEVELOPMENT OF A
WIDTH-MODULATED PULSE REBALANCE
ELECTRONICS LOOP FOR STRAPDOWN GYROSCOPES
(Tennessee Univ.) 65 p HC \$5.25

N73-28649

Unclas
CSCL 17G G3/21 15268

DEVELOPMENT OF A WIDTH-MODULATED PULSE REBALANCE ELECTRONICS
LOOP FOR STRAPDOWN GYROSCOPES

Reproduced by
NATIONAL TECHNICAL
INFORMATION SERVICE
US Department of Commerce
Springfield, VA. 22151

Prepared for George C. Marshall Space Flight Center, National Aeronautics
and Space Administration under Contract NAS8-27296/DCN 1-1-40-10230

THE UNIVERSITY OF TENNESSEE

DEPARTMENT OF ELECTRICAL ENGINEERING



Scientific Report S-25
July 13, 1973

DEVELOPMENT OF A WIDTH-MODULATED PULSE REBALANCE
ELECTRONICS LOOP FOR STRAPDOWN GYROSCOPES

Prepared For
George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Under Contract NAS8-27296/DCN 1-1-40-10230

T. V. Blalock, E. J. Kennedy, and R. D. McKnight

Department of Electrical Engineering
The University of Tennessee
Knoxville, Tennessee 37916

ACKNOWLEDGEMENTS

The authors are grateful for the generous assistance of the staff of the Astrionics Laboratory, MSFC, during the work reported in this paper. The encouragement and advice of Dr. G. B. Doane, III, Mr. B. J. Doran, Mr. Joe Parker, Mr. Harry Reid, and Mr. Hugo Berry are especially appreciated. The authors thank Dr. James C. Hung, Project Director, for his efforts in the administration of the project.

Mr. Gene Fendley, graduate student, Mr. Mike Galyon and Mr. Jerry Norton, undergraduate students, were very helpful in the fabrication and evaluation of several sections of the breadboard.

The skillful preparation of the manuscript by Mrs. Mary Moore is very much appreciated.

TABLE OF CONTENTS

SECTION	PAGE
I. INTRODUCTION	1
II. DESIGN THEORY.	3
Development of the System Transfer Functions.	3
Loop Design Constraints	8
Limit Cycle Ripple	8
Ramp Slope Constraint.	9
Random Noise	10
Amplifier Saturation	11
Quantization Error	12
Sampling Theorem	12
Data Resolution.	13
Synthesis of the System Loop Transmission	13
Loop Transmission of the 2544 Gyro	14
Loop Transmission of the GG334 Gyro.	16
Transfer Function Distribution.	18
Kearfott 2544 Gyro	18
Honeywell GG334 Gyro	21
III. DESIGN IMPLEMENTATION.	22
AC Amplifier.	22
Synchronous Demodulator	22
DC Amplifier and Loop Compensation.	28
Duty Cycle Generator.	31
Torque Current Generator.	31

SECTION	PAGE
Precision Voltage Reference.	32
Comparator Operational Amplifier	33
Error Amplifier.	35
Power Transistor Stage	36
H-Switch	36
H-Switch Driver.	37
Sampling Resistors	38
Interfacing Network.	39
Torquer Compensation	39
Versatility of the Generator	41
Reduction of Number of Power Supplies.	41
Logic	42
CMOS Crystal Controlled Clock	43
Pickoff Excitation Signal Generator	47
Spin Motor Power Supply	49
IV. EXPERIMENTAL RESULTS	52
Honeywell GG33 ⁴ Gyro.	52
Kearfott 25 ⁴ ₄ Gyro.	54
V. PROPOSED WORK.	58

INTRODUCTION

A new width-modulated pulse rebalance electronics loop was developed for use with strapdown gyroscopes. The decision to develop a width-modulated binary loop was based on the study reported last year¹ in which a width-modulated and a ternary loop were compared, and also on additional results obtained in the first phase of the work reported here. The salient advantages of the width-modulated binary over the ternary loop which strongly influenced our decision are the following: (1) the H-switch is easier to implement, (2) torque is applied in finely quantized increments, (3) the analog-to-digital conversion for data generation is inside the loop and is directly determined by the torque pulse, (4) no part of the loop compensation network bypasses the gyroscope, and (5) the torquer is fed constant power.

The basic design goals for the new rebalance loop were (1) versatility for accomodating a number of different gyros with minimum change in loop parameters, (2) minimization of required number of power supply voltages, (3) at least a factor-of-two increase in error signal sampling rate, (4) improved performance with special emphasis on reduction of uncertainties in data output due to all sources of noise, (5) a wide range of available scale factors, (6) reduction of system complexity for improved reliability, and (7) amenability to microcircuit implementation.

The design theory needed to synthesize the rebalance loop is developed in the first section of this report. The details of the implementation of each part of the loop are discussed in the second section. Some results of the experimental evaluation of a breadboard of the rebalance loop are

reported in the third section. The final section of the report contains some summarizing comments, observations, and proposals for future work.

DESIGN THEORY

The general design equations for the synthesis of a width-modulated binary rebalance loop will be developed in this section. The basic transfer function and design constraint equations will be derived. These will then be used to synthesize the loop transmission in frequency space for the Honeywell GG334 and the Kearfott 2544 gyroscopes. Finally, the actual system transfer functions for each of the two gyros will be determined to both satisfy the loop transmission requirements and the design constraints caused by random noise, limit cycle ripple, saturation effects, etc.

Development of the System Transfer Functions

The basic elements of the rebalance electronics loop are depicted in Fig. 1. The gyro transfer function H_{tgp} operates on an average torque-current (mA) to generate an ac voltage output of magnitude V_p when the rate input to the gyro is zero. The input to the gyro float is a torque and the output is an angular displacement so that the float transfer function becomes

$$H_g = \frac{1}{Js^2 + Fs + B}, \text{ (rad/dyne-cm)} \quad (1)$$

where J is the float inertia in gm-cm^2 , F is the damping coefficient in dyne-cm-sec and B is the elastic restraining torque in dyne-cm . If the elastic restraint is small and a characteristic time τ_g is defined as $\tau_g = J/F \text{ sec}$,

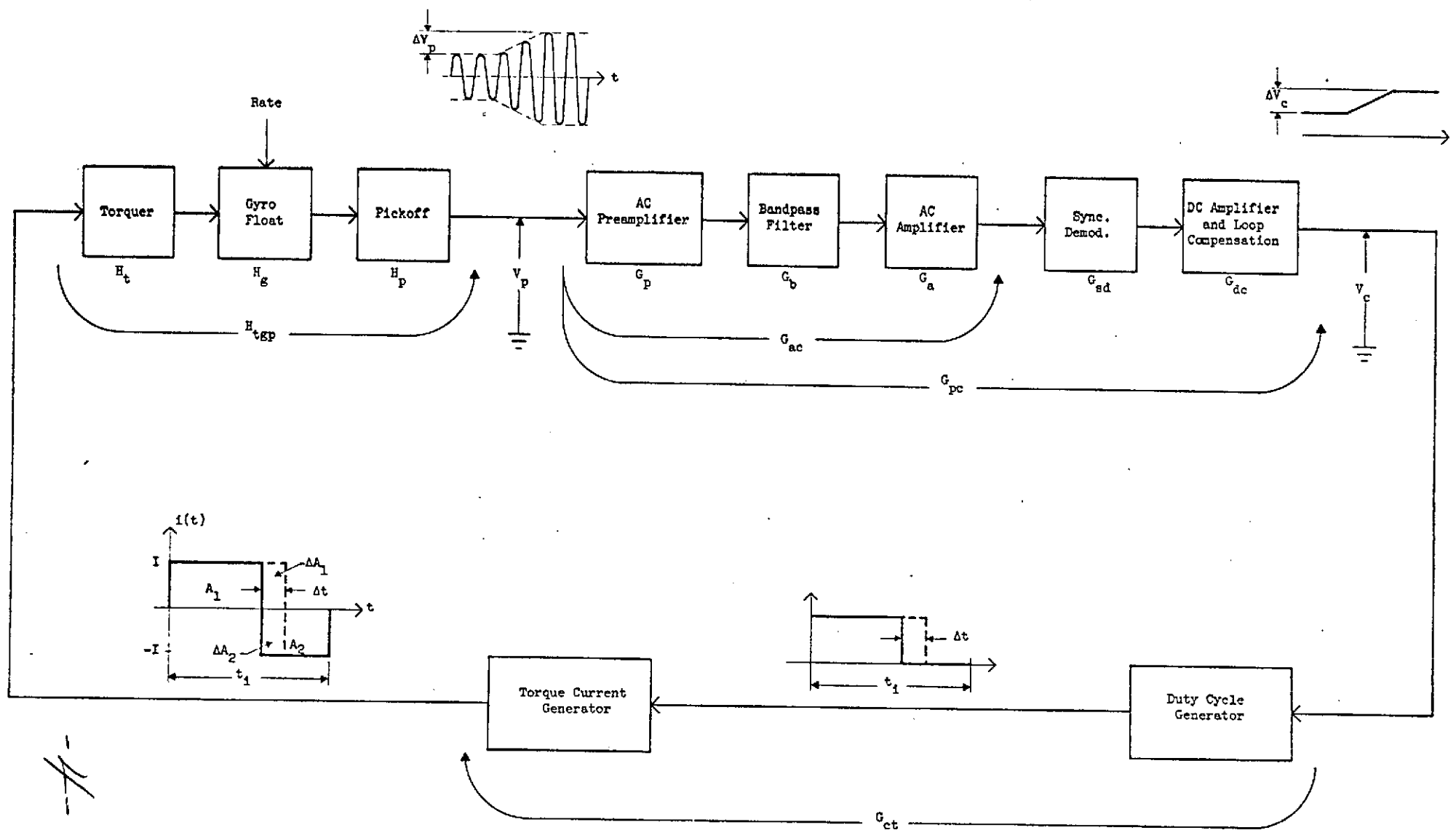


Fig. 1. The Basic Elements of a Width-Modulated Binary Rebalance Loop.

$$H_g \approx \frac{1}{Fs(1 + \tau_g s)} \quad (2)$$

The torquer transfer function is given approximately by

$$H_t = \frac{K_t F}{1 + \tau_t s} \frac{2\pi}{360} \quad (\text{dyne-cm/mA}) \quad (3)$$

where K_t is the torquer scale factor in degrees/sec-mA, and τ_t is the torquer time-constant which is usually sufficiently low (especially for a compensated torquer) relative to other system time-constants to be negligible.

The input to the pickoff is an angular displacement in radians which generates an output voltage ΔV_p volts. If the pickoff scale factor is given in K_p volts/degree, then

$$H_p = K_p \frac{360}{2\pi} \quad \text{volts/rad.} \quad (4)$$

The overall gyroscope transfer function now becomes (see Fig. 1)

$$H_{tgp} = H_t H_g H_p$$

$$H_{tgp} = \frac{K_t K_p}{S(1 + \tau_g s)} \quad \text{volts/mA} \quad (5)$$

where the torquer time-constant has been assumed to be very short.

The transfer function G_{ac} of Fig. 1 can be designed to have negligible phase shift in the frequency range where the system loop transmission has a magnitude greater than unity. The preamplifier must have high common

mode rejection and should control the uncertainty due to random noise. The bandpass filter G_b discriminates against unwanted signals. The amplifier G_a provides additional gain and is used to switch system gain as the torque current level is changed to accommodate different gyro rate inputs. The gain of the synchronous demodulator is usually set near unity and can be designed to contribute negligible phase shift.

The loop transmission frequency response is shaped in the block G_{dc} . Usually two poles and one zero in the G_{dc} transfer is adequate. The location of those poles and the zero in the s -plane depends on (1) the gyro transfer function, (2) stabilization against self-oscillations in the loop, (3) discrimination against noise signals, and (4) desired closed loop bandwidth for the system.

The overall transfer function $G_{pc} = G_{ac} G_{sd} G_{dc}$ is the ratio of the change ΔV_c in the voltage level V_c to a change ΔV_p in the amplitude of the pickoff output sinusoid as shown in Fig. 1. The general expression for the transfer function is

$$G_{pc} = K_{pc} \frac{1 + s\tau_z}{(1 + s\tau_{p1})(1 + s\tau_{p2})} \quad (\text{volts/volt}) . \quad (6)$$

The voltage V_c is mixed with a ramp signal R volts/sec in the duty cycle generator (Fig. 1) and then the crossing of a fixed voltage level is detected to properly distribute the positive and negative torque current over the interrogation period t_i . Since the time t_i is chosen to be small relative to the gyro time-constants, the gyro essentially integrates the torque current. Thus the input of interest to the gyro block H_{tgp} is the average current I_{av} .

The average current is given by

$$I_{av1} = \frac{1}{t_i} \int_0^{t_i} i(t) dt = \frac{A_1 - A_2}{t_i},$$

as shown in Fig. 1. In like manner

$$I_{av2} = \frac{A_1 + \Delta A_1 - (A_2 - \Delta A_2)}{t_i},$$

$$\Delta I_{av} = I_{av2} - I_{av1} = \frac{2\Delta A}{t_i},$$

since $\Delta A = \Delta A_1 = \Delta A_2$ when $|+I| = |-I|$.

But $\Delta A = I\Delta t$; therefore,

$$\Delta I_{av} = \frac{2I\Delta t}{t_i}.$$

The time increment is determined by the ramp slope R and is

$$\Delta t = \frac{\Delta V_c}{R}.$$

Then we have for the transfer function G_{ct}

$$G_{ct} = \frac{\Delta I_{av}}{\Delta V_c} = \frac{2I}{Rt_i}, \text{ (mA/volt)}. \quad (7)$$

where I is in mA.

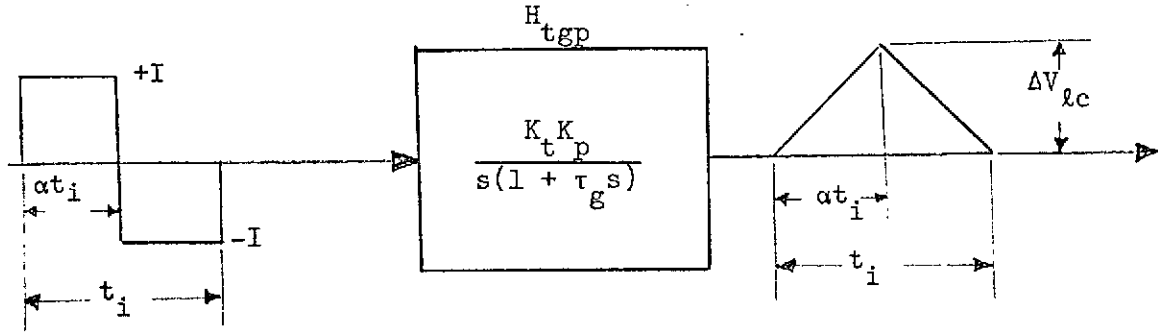
The loop transmission for the system now becomes

$$G_l = H_{tgp} G_{ac} G_{ct}$$

$$G_l = \frac{2K_t K_p K_{pc} I (1 + s\tau_z)}{R t_i s(1 + \tau_g s)(1 + s\tau_{p1})(1 + s\tau_{p2})} \quad (8)$$

Loop Design Constraints

Limit Cycle Ripple. The gain of the ac amplifier G_{ac} is constrained by the limit-cycle ripple that appears at the pickoff output. The worse



case condition occurs when $\alpha = \frac{1}{2}$ and $\tau_g = 0$ in the figure above. The peak-to-peak limit cycle output voltage ΔV_{lc} can be estimated from

$$\Delta V_{lc} = \int_0^{\frac{t_i}{2}} K_t K_p I dt.$$

Thus, the maximum limit-cycle ripple is

$$\Delta V_{lc} = \frac{K_t K_p I t_i}{2} \quad (9)$$

For a specific gyro, Eq. (9) must be considered when the gain of the ac amplifier is chosen to avoid saturation of the amplifier output.

Ramp Slope Constraint. For proper operation of the duty cycle generator, the slope of the internal ramp signal that is mixed with the amplifier error signal V_c (Fig. 1) must be greater than the maximum possible slope of the error signal. That is

$$R > \left. \frac{dV_c}{dt} \right|_{\text{max.}} . \quad (10)$$

The slope of the error signal is controlled primarily by the gyro dynamics. For maximum torque rate at a torque current of value I , the voltage $V_c(t)$ is given by

$$V_c(t) = K_{pc} \int_0^t K_t K_p I dt , \quad (11)$$

$$\frac{dV_c(t)}{dt} = K_{pc} K_t K_p I . \quad (12)$$

Equation (12) gives the worse case slope (maximum slope) since only the gyro integrating time-constant is assumed to be limiting the slope and also it is assumed that I is being applied continuously. However, we will insist for any specific gyro that

$$R > K_{pc} K_t K_p I , \text{ (volts/sec.)} . \quad (13)$$

where I is in mA.

The design inequality (13) leads to some interesting constraints on the magnitude of the loop transmission at low frequencies and on the maximum system bandwidth. From Eq. (8) and inequality (13),

$$G_{\ell} \Big|_{\text{low freq.}} < \frac{2}{j\omega t_i}, \quad (14)$$

or

$$|G_{\ell}| \Big|_{\text{low freq.}} < \frac{1}{\pi f_{\ell} t_i} = \frac{f_i}{\pi f_{\ell}}. \quad (15)$$

The low frequency region where f_{ℓ} exists is in the -6 db/octave slope of the loop transmission caused by the gyro integration; thus, f_{ℓ} is lower than any of the 3 db frequencies of the compensation network.

If the high frequency region of the loop transmission has a slope of -6 db/octave or greater, then the maximum possible closed-loop bandwidth of the rebalance loop is given by

$$f_{\text{cl}} \Big|_{\text{max.}} = \frac{f_i}{\pi} = \frac{\text{limit-cycle frequency}}{\pi}. \quad (16)$$

Random Noise. It is important to know the rms value of the system random noise at the duty cycle generator input; the value should be sufficiently low to produce less than one data pulse uncertainty. Good design practice requires the random noise from the electronics to be caused almost entirely by the preamplifier. A preamplifier voltage gain of about 10 will usually force this condition.

If the voltage ΔV_{cq} is the increment in voltage applied to the duty cycle generator that produces a one data pulse increment in the data train, the rms value of the random noise at the input to the duty cycle generator should be less than ΔV_{cq} volts rms. The constraint on the equivalent noise voltage spectral density at the preamplifier input becomes

$$ENV_p \Big|_{f=f_p} < \frac{\Delta V_{cq}}{(\Delta f_n)^{1/2} G_{pc} \Big|_{f=f_p}}, \text{ (volts/Hz}^{1/2}\text{)} \quad (17)$$

where Δf_n is the noise bandwidth of the bandpass filter, $G_{pc} \Big|_{f=f_p}$ is the magnitude of the transfer function $G_{pc}(j\omega)$ at the pickoff excitation frequency f_p . The right hand side of inequality (17) is only an estimate, since an exact calculation would have to account for the rather complex processing of the random noise by the synchronous demodulator.

It is not always easy to force the preamplifier to control the random noise. The distribution of gain and filtering in the G_{pc} block (Fig. 1) should be accomplished with the effects of the distribution on random noise always clearly in mind. Usually, the uncertainties due to random noise are negligible relative to other uncertainties in the system.

Amplifier Saturation Constraints Due to Gyro Float Dynamic Range. If the ac amplifier block G_{ac} is not carefully designed for overload performance, saturation of the amplifier for large excursions of the gyro float from the null position may shift the phase of the output signal more than 90° with a consequent reversal of the synchronous demodulator output and latchup of the rebalance loop. A reasonable design constraint is to require less

than 45° phase shift in the G_{ac} block output for a float excursion from the null position to either stop. This constraint usually requires special overload circuits and influences the gain distribution in the G_{ac} block.

Quantization Error Constraint. All the uncertainties generated in the system when combined at the duty cycle generator input should be less than ΔV_{cq} , the voltage quantization, to keep the data error less than one data pulse. One of the first steps in synthesizing a rebalance loop for a specific gyro is to calculate the numerical value for ΔV_{cq} .

The general expression for ΔV_{cq} can be found as follows: If the data rate is R_d pulses per second, then the number of pulses per interrogation period is $R_d t_i$. The total voltage excursion of the ramp in one interrogation period is $R t_i$ volts. Thus, the voltage quantization is

$$\Delta V_{cq} = \frac{R t_i}{R_d t_i},$$

$$\Delta V_{cq} = \frac{R}{R_d} \text{ (volts/data pulse)}. \quad (18)$$

The voltage quantization is fixed by the ramp rate and the data rate.

Sampling Theorem Constraint. The maximum closed-loop bandwidth of the rebalance loop is limited by the rate at which the amplified error signal is sampled as well as by the result expressed by Eq. (16). The sampling frequency is just the limit-cycle frequency f_i . Since the highest frequency that can occur in the error signal is approximately equal in value to the 3 db bandwidth of the closed-loop system, then the sampling theorem requires that

$$f_{cl} < \frac{f_i}{2} \quad (19)$$

It is clear that the constraint or bandwidth set by Eq. (16) is controlling.

Data Resolution. The data resolution of the rebalance loop depends on the gyro torquer scale factor and on the smallest increment in torque current area that can be generated by the duty cycle generator. The limit cycle is incremented by a synchronizing pulse train (see ref. 1). The limit cycle gates this same pulse train to produce a data train each interrogation period, t_i . The number of pulses in the data train is proportional to the net torque current area generated in that period t_i .

For a data rate of R_d pulses per second, the smallest torque-current area increment is

$$\Delta A_q = \frac{2I}{R_d}.$$

The data resolution $\Delta\theta_d$ is the smallest torque-current area increment multiplied by the torquer scale constant K_t ; thus,

$$\Delta\theta_d = \frac{7200 K_t I}{R_d} \text{ (arc-sec)}, \quad (20)$$

where K_t is in degrees/mA-sec and I is in mA.

Synthesis of the System Loop Transmission

The beginning point in the detailed design of a width-modulated binary rebalance loop in the configuration of Fig. 1 is to synthesize the loop transmission of the system. We will develop the details of the loop transmission in frequency space using the familiar Bode diagram. The

loop transmission for the Kearfott 2544 and the Honeywell GG334 gyroscopes will be synthesized in the following sections.

Loop Transmission for the 2544 Gyroscope. The characteristics for the 2544 gyro needed for the loop transmission design are listed in Table I.

TABLE I - Gyroscope Characteristics

Characteristic	Symbol	2544	GG334	Units
Spin Motor Excitation Frequency		800	800	Hz
Spin Motor Speed		24,000	24,000	rpm
Torquer Scale Factor	K_t	0.57	0.28	degree/mA-sec
Pickoff Scale Factor	K_p	0.22	0.35	volts/degree
Characteristic Time	τ_g	0.26	0.5	msec
Sig. Gen. Frequency	f_{ex}	19.2	32	kHz
Sig. Gen. Excitation		8	5	volts rms

A design goal was to at least double the sample rate (halve the interrogation period) of the fastest width-modulated binary loop^{1,2} available at the initiation of our development work. That rate was 1 kHz. We selected a rate of 2.4 kHz for the 2544 gyro to satisfy the design goal and also be compatible with the synchronizing of the 19.2 kHz pickoff excitation frequency f_{ex} and the 800 Hz spin motor power supply. The clock was chosen to be 2.4576 MHz and was scaled down to a 614.4 kHz pulse train to be used for both data generation and synchronization of logic functions and duty-cycle generator outputs.

Each interrogation period t_i was divided therefore, into 256 increments with a consequent data resolution of [Eq. (20)]

$$\Delta\theta_d = \frac{(7200)(.57)(30)}{614.4 \times 10^3} = 0.2 \text{ arc-sec} ,$$

where I was taken as 30 mA which was the lowest value selected for torque current.

The low frequency region of the Bode diagram is determined by the ramp slope constraint expressed by inequality (15). A reasonable design criterion is to set the ramp slope equal to twice the maximum error signal slope. Thus, the magnitude of the loop transmission at $f = f_\ell = 0.1 \text{ Hz}$ is

$$|G_\ell|_{\text{low freq.}} = \frac{f_i}{2\pi f_\ell} = 3830 ,$$

$$|G_\ell|_{.1\text{Hz}} = 71.7 \text{ db.} \approx 72 \text{ db}$$

The 6 db/octave slope of the Bode plot due to the gyro integration must pass through the 72 db gain point at $f = 0.1 \text{ Hz}$.

The high frequency region of the loop transmission is determined by closed loop bandwidth requirements. For gas bearing gyros, vibrations at one-half the wheel frequency may occur² and should be discriminated against by proper shaping of the high-frequency portion of the loop transmission. Hamilton Standard² used the criterion that the loop transmission should be down -20 db at one-half the wheel frequency. Although the 2544 gyro was a ball bearing type, we adopted the -20 db design criterion since our system

will also be used with the GG334 gas bearing gyro. Therefore, a point at $|G_\ell| = -20$ db and $f = 200$ Hz was set.

The loop transmission between $f = 0.1$ Hz and 200 Hz was shaped with the two poles and one zero of the compensator to give high loop transmission magnitude with sufficient phase margin for stability against closed-loop self oscillations. The resulting Bode diagram is shown in Fig. 2.

The loop transmission magnitude of Fig. 2 crosses the 0 db line at 40 Hz; hence, the closed loop bandwidth f_{cl} should be 40 Hz. The compensation network must contain a pole at 1 Hz, a pole at 100 Hz, and a zero at 10 Hz. The phase margin at the 0 db crossing is about 42° and at the maximum phase shift region of the -12 db/octave slope between 1 Hz and 10 Hz, it is about 35° (at $f \approx 3.2$ Hz).

Loop Transmission for the GG334 Gyroscope. The parameters of the GG334 gyro indicate that the loop transmission of Fig. 2 can also be used for it. The pole due to the higher characteristic time τ_g is lower (320 Hz compared to 610 Hz) than that of the 2544; however, in both cases the effect of τ_g is negligibly small for the pole-zero constellation chosen for the compensator.

A modification of the logic signal frequencies will be necessary for the GG334 gyro because of the 32 KHz pickoff excitation. A clock frequency of 4.096 or 2.048 MHz will scale down to produce a 512 KHz data train, and a 32 KHz pickoff excitation. However, these frequencies will not allow generation of a proper sync signal by simple binary division for the 800 Hz spin motor power supply. It is suggested, therefore, that the logic signals for the 2544 gyro also be used for the GG334 gyro. This

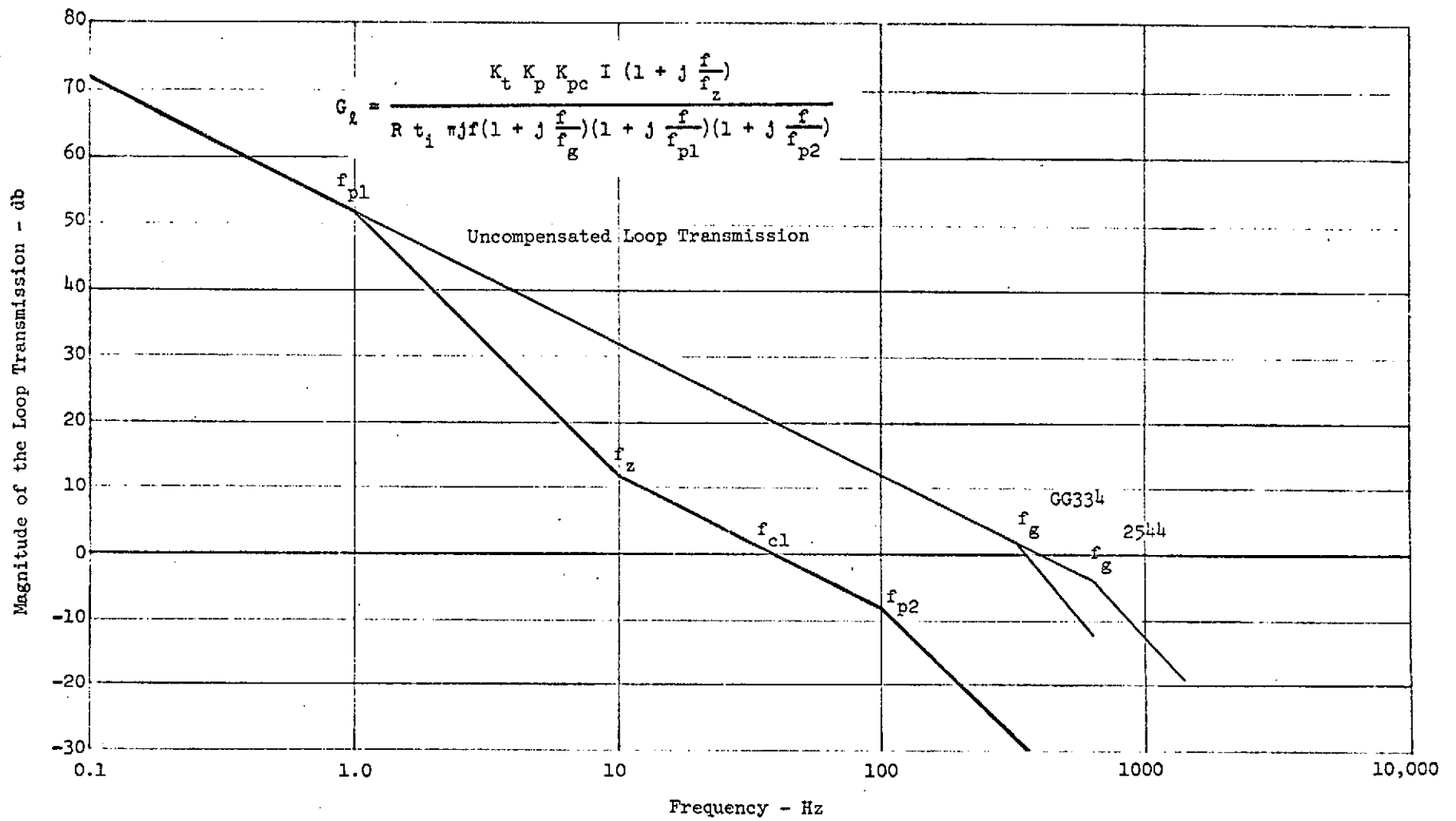


Fig. 2. Loop Transmission

will require either a 19.2 kHz or a 38.4 kHz excitation voltage for the GG334 pickoff. If the excitation signal must be 32 kHz, then a more complex divider must be used for obtaining the synchronizing signals.

The distribution of transfer functions in the rebalance loop will be slightly different for the two gyroscopes; this part of the development will be considered in the next section.

Transfer Function Distribution to Achieve the Required Loop Transmission

Kearfott 2544 Gyroscope. The low-frequency loop transmission was set at 3830 at $f = 0.1$ Hz for a ramp slope twice the maximum error signal slope at the input to the duty cycle generator. A ramp slope of 10^4 volts/sec was chosen for compatibility with the TTL logic functions now being used in our duty cycle generator. The maximum value of K_{pc} (Eq. 8 and Fig. 1) is required for the smallest value of torque current which was chosen to be 30 mA. Thus, from Eq. (8)

$$K_{pc} = \frac{(3830)(10^4)(417 \times 10^{-6})(2\pi)(.1)}{(2)(.57)(.22)(1)},$$

$$K_{pc} = \frac{4 \times 10^4}{I}, \quad (21)$$

$$K_{pc}^{30mA} = 1330. \quad (22)$$

The proper distribution of the gain K_{pc} in the section G_{pc} (Fig. 1) of the loop transmission depends on signal-to-noise ratio requirements and saturation effects. The gain of the ac preamplifier should be high enough to control the electronic noise performance of the system but not high

enough to saturate should the gyro float be moved to the mechanical stops. For the 2544 gyro, a gain $G_p = 20$ will suffice.

Since most of the gain should precede the synchronous demodulator to minimize the noise contributions of the demodulator and the compensator, a gain of about 4 at low frequencies was chosen for the product $G_{sd} G_{dc}$. The synchronous demodulator gain was set to $\pi/2$ so that a 1 volt peak sinusoidal input would produce a 1 volt dc output. The gain G_{dc} then must be 4 at low frequencies.

The bandpass filter is a two section active resistance-capacitance filter with a low Q of 0.87 for each section to give small phase shift with shifts in excitation frequency or normal aging of components. The center frequency gain of the bandpass filter was set to about 1.7. The skirts have slopes of about 12 db/octave. The gain of the ac amplifier G_{ac} was therefore required to be about 10.

To maintain constant loop transmission for different scale factors, the gain must be switched somewhere in the loop. The ac amplifier is a convenient place to perform this function; it was designed to operate over a gain range of 1 to 25 which allows a wide range of scale factor selection. Special overload circuits that were incorporated in the ac amplifier to accomodate this wide gain range will be discussed in later sections of this report.

The maximum limit cycle ripple at the ac preamplifier input calculated from Eq. (9) is 3.93 mV for the maximum torque current of 150 ma. At the preamplifier output, the maximum limit cycle ripple would produce about 77 mV of amplitude modulation on the error signal. Most of this ripple would be carried in sidebands at 19.2 ± 2.4 kHz. Since the Q of the bandpass

filter is low, there will be little attenuation of the ripple. The maximum ripple at the output of the bandpass filter would be about 131 mV. Because of the gain switching function of the ac amplifier, the 2.4 kHz ripple at its output would never exceed 262 mV which is well within the linear range of the ac amplifier.

The limit cycle ripple at the input to the duty cycle generator must not exceed the voltage quantization given by Eq. (18).

$$\Delta V_{cq} = \frac{10^4}{6.144 \times 10^5} = 16.3 \text{ mV} . \quad (23)$$

The maximum ripple peak-to-peak voltage at the compensator output can be estimated from the compensator transfer function (see Eq. 8).

$$\Delta V_{2.4 \text{ kHz}}^{\max} = \frac{(4) \left(\frac{2.4 \times 10^3}{10} \right)}{\left(\frac{2.4 \times 10^3}{1} \right) \left(\frac{2.4 \times 10^3}{100} \right)} (262 \text{ mV})$$

$$\Delta V_{2.4 \text{ kHz}}^{\max} = 4.37 \text{ mV} .$$

Thus, the maximum expected uncertainty due to the limit cycle ripple is about 1/4 data pulse.

The compensator constrains the noise bandwidth of the G_{pc} section to extend from 0 to about 2 Hz. This is a very narrow noise bandwidth but since the synchronous demodulator enhances low frequency noise, we will calculate the equivalent noise voltage spectral density at the preamplifier input that would produce an uncertainty of ΔV_{cq} volts rms. This is

$$\text{ENV} = \frac{16.3 \text{ mV}}{1330 \sqrt{2}} = 8.67 \text{ } \mu\text{V/Hz}^{1/2}, \quad (24)$$

which is an extremely high value. The low-frequency electronic noise generated in the preamplifier is greatly attenuated by the bandpass filter since the noise should not amplitude modulate the error signal f_{ex} but rather be linearly mixed with it. Thus, electronic noise from the G_{ac} section should produce negligible uncertainty at the duty cycle generator input.

Honeywell GG334 Gyroscope. If the excitation signal frequency for the GG334 gyro can be set at 19.2 kHz, the only change necessary in the 2544 rebalance loop is to increase the gain of the ac amplifier G_a of Fig. 1. Since the $K_t K_p$ product for the 2544 gyro is 28% higher than for the GG334 gyro, a 28% increase in G_a will allow essentially the same loop transmission for the GG334 as for the 2544. This gain increase can be accomplished by changing only one resistor in the ac amplifier.

If the excitation frequency for the GG334 gyro must be 32 kHz, then the bandpass filter center frequency must be changed. This is easily accomplished by changing four resistors in the bandpass filter. In addition, some modification of the logic dividers would be necessary to obtain the synchronizing signals for the pick-off excitation signal and spin motor power supply.

DESIGN IMPLEMENTATION

A block diagram of the rebalance electronics for the Kearfott 2544 gyroscope is shown in Fig. 3. Some details of the power supply distribution and grounding are indicated in the figure. Separate twisted wires (+ supply lines, - supply lines, and power ground) were run to (1) the ac preamplifier, (2) the bandpass filter and ac amplifier last stage, (3) dc amplifier and compensator, (4) duty cycle generator, (5) torque current generator, and (6) logic. There are two separate grounds, "A" and "B" which are connected on the duty cycle generator board and at a common ground point for all the power supplies. The ground line in each twisted set of wires emanates from the common power supply ground. The spin motor and pickoff excitation are all synchronized with the limit cycle; this is essential to minimize data pulse splatter.

The logic supply voltage is designated "+L"; it will be +5 volts for TTL logic and +10 volts for CMOS logic.

The implementation considerations and a description of each block in the system of Fig. 3 will be discussed in this section. Each block indicated in Fig. 3 occupies a separate board (the ac amplifier is on a single board).

AC Amplifier

The Analog Devices AD-520 was selected for the ac preamplifier primarily because of its very high common-mode rejection ratio - greater than 100 db below 100 Hz for a differential gain of 20. Even at 100 kHz, the CMRR is greater than 40 db. The high slew rate, > 2.5 volts/ μ sec, is also necessary to avoid phase shifts for large signals. The random noise ENV of the preamplifier at low frequencies (dc-10 Hz) is about $0.3 \mu\text{V}/\text{Hz}^{1/2}$. The rejection

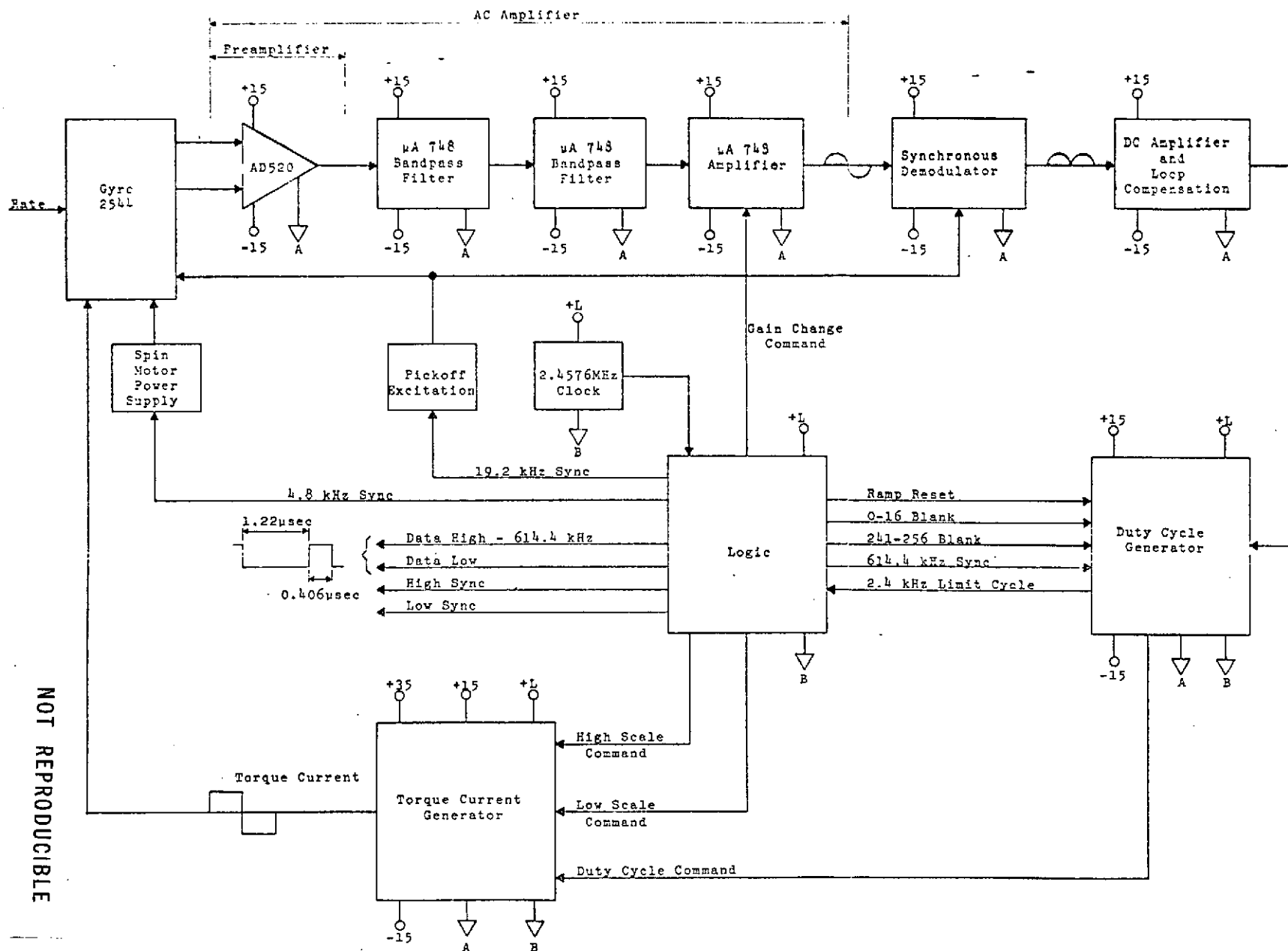


Fig. 3. U.T. Rebalance Electronics - Block Diagram.

of this noise by the bandpass filter will cause the effective ENV of the preamplifier to be much less than $0.3 \mu\text{V}/\text{Hz}^{1/2}$ which is much below the value of $8.67 \mu\text{V}/\text{Hz}^{1/2}$ [Eq. (24)] that would produce an rms uncertainty of ΔV_{cq} (one data pulse).

The active bandpass filter is a two stage operational amplifier resistance-capacitance filter with center frequency f_o at 19.2 KHz, 12 db/octave slopes, $Q \approx 0.9$, and gain about 1.7. The feedback parameters were selected from the following relationships³

$$R_1 = \frac{Q}{H_o \omega_o C},$$

$$R_2 = \frac{Q}{(2Q^2 - H_o) \omega_o C},$$

$$R_5 = \frac{2Q}{\omega_o C}, \quad (25)$$

where ω_o is the center frequency, H_o is the voltage gain at the center frequency, and the resistors and capacitors are identified in Fig. 4. The 200 pF capacitor C_4 in the second stage of the bandpass filter A3 provides feedforward around lateral pnp transistors in the operational amplifier to reduce large signal phase shift, and increase the amplifier slew-rate.

The output stage of the ac amplifier is designed to accommodate a range of gain requirements and also provide gain switching facility for scale factor changes. The Q1-Q2 clamp circuit in the feedback path of A4 minimizes phase shifts under overload conditions. The MOSFET switch Q3 in the gain change circuit allows a logic signal to switch gain with minute current

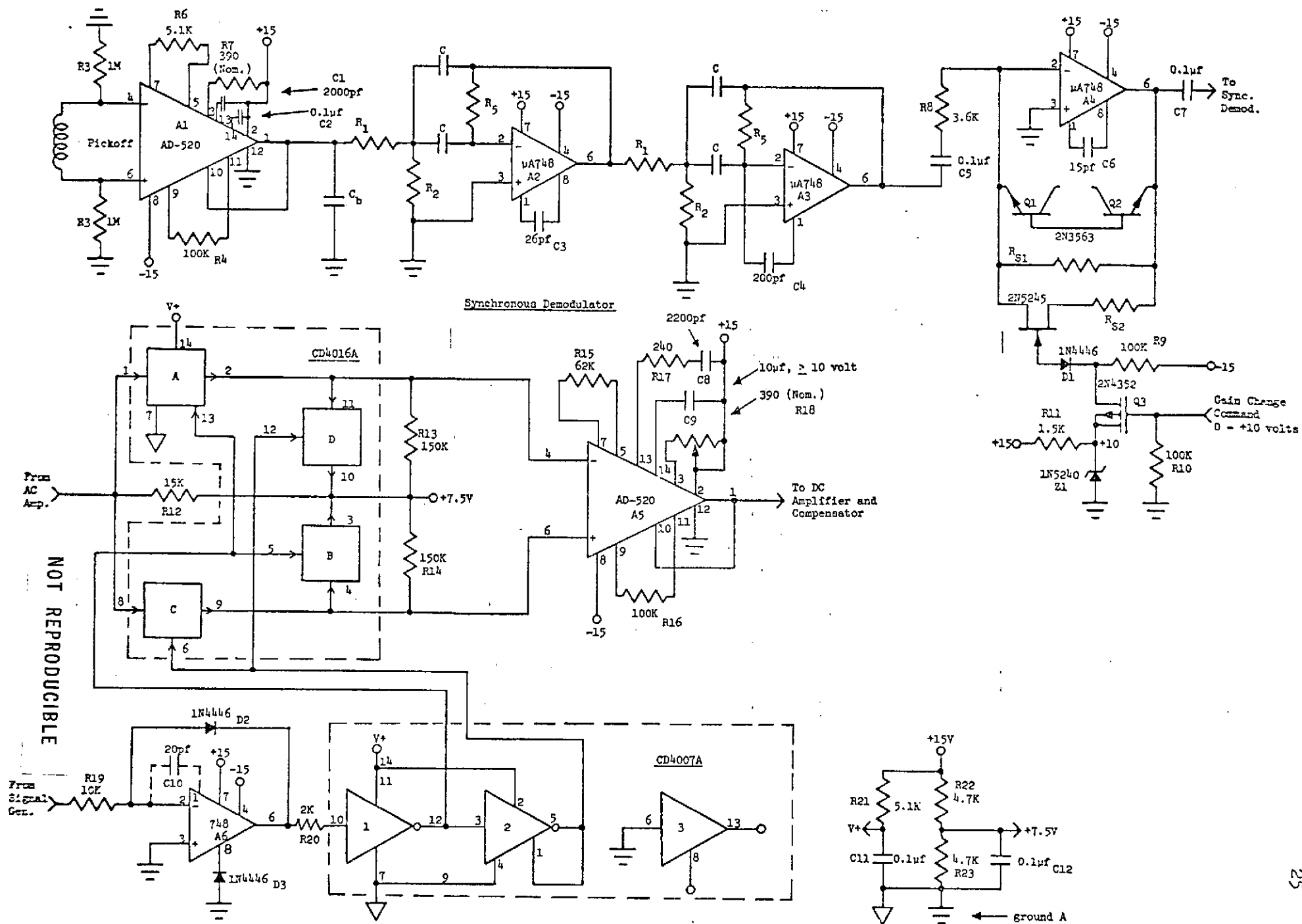


Fig. 4. AC Amplifier and Synchronous Demodulator

flow; this is essential to prevent logic current contamination of the amplified error signal.

The emphasis on the minimization of phase shift in the ac amplifier was necessary to assure that the loop could not be moved into a positive feedback region by the operation of the synchronous demodulator on the amplified pickoff signal. A phase shift of more than 90° in the ac amplifier (perhaps due to a saturated output) could produce the positive feedback situation with a consequent latchup of the loop.

Synchronous Demodulator

The synchronous demodulator converts a sinusoidal AC input to a dc output, with the correct phase as determined by the signal generator. The dc output of the demodulator must be linearly related to the peak value of the ac input.

The circuitry for the synchronous demodulator is indicated in Fig. 4. The AD520 instrumentation amplifier A5 replaces a typical differential connection of three - 748 amplifiers. The input ac signal is full-wave rectified by the gating signal from the CD4007A inverters which allow half the sinusoid to be amplified by the inverting input and the other half by the non-inverting input of the AD520. These lobes are then summed at the output, and applied to the DC amplifier and compensator group. The use of the CMOS CD4016A quad bilateral switch provides equal linearity and reduction of gating transients through both inputs of A5. This switch is connected in a complementary configuration, such that when switches A and B are ON, then C and D are OFF, and vice-versa. Since the CMOS logic is connected from +15V to ground, the quad switches were raised to a common-mode voltage of +7.5V, which allows an

input AC signal of 7.5V peak.

The synchronous gating signal is obtained by the sinusoidal output of the signal generator. The 748 amplifier (A6) is connected as a zero-crossing detector, and converts the sinusoid to a synchronous -0.5 to 15V square-wave signal to drive the CD4007A inverters. Resistor R20 is included to limit the current through the protective input diode of the CD4007A-1 inverter, should the lower output level (-0.5V) of A6 exceed the diode threshold. If the entire logic were CMOS, one could eliminate amplifier A6 and obtain a synchronous square-wave signal directly from the logic output that drives the signal generator.

For a full wave rectified signal, the dc value is equal to $2E_{\max}/\pi$, where E_{\max} is the peak value of the AC input signal. For convenience, the gain of the synchronous demodulator was chosen as unity, hence the gain of A5 was set equal to $\pi/2$ (i.e., the ratio is approximately 100K/62K).

One of the primary advantages obtained by the use of the CMOS bilateral switch as a gating element is the isolation of the drive signal from the amplified error signal of the loop, that is not obtained by the use of typical bipolar transistor demodulators. Also, since all four switches are on the same monolithic chip, the "on" resistance in each input side of A5 is the same.

The AD520 amplifier A5 requires a frequency compensation network of 2200pf and the series 240-ohm resistor. The output dc zero (for no AC signal input) can be balanced by a 1K potentiometer (R18) from pins 2 to 3. However, since this amplifier is after a large AC gain, this adjustment is not absolutely required, and could therefore be replaced by a 390-ohm resistor connected between pins 2 and 3. The 10 μ f capacitor C9 could also be

replaced by a 0.1μf, or 0.01μf capacitor, at the expense of increased flicker noise in the loop.

DC Amplifier and Loop Compensation

The dc amplifier section follows immediately after the synchronous demodulator. Its function is to provide the remaining electronic gain and to shape the overall rebalance loop transmission for adequate system stability. These functions are obtained by the amplifiers A1 and A2, and their associated networks, in Fig. 5. As was developed earlier in the design section, the dc amplifier must provide a gain of approximately 4, while the loop must be shaped by the addition of two poles and one zero. In Fig. 5 the voltage transfer function of the A1 amplifier block is

$$\frac{V_{o1}}{V_{i1}} = -\left(\frac{R3}{R4}\right) \left(\frac{R1 + R2}{R2}\right) \frac{1 + SR5 C2}{1 + SC2 [R5 + R3(1 + R1/R2)]} , \quad (26)$$

while the transfer function of the A2 block is

$$\frac{V_{o2}}{V_{i2}} = \frac{V_{o2}}{V_{o1}} = -\left(\frac{R9}{R7}\right) \left(\frac{1}{1 + SR9 C3}\right) , \quad (27)$$

where it has been assumed that the bandwidth of the amplifiers A1 and A2 are much greater than the pole and zero locations of Eqs. (26) and (27). The pole location of Eq. (27) could also have been obtained with amplifier A1 by placing a capacitor from the center of R4 to ground. This would require, however, a considerable increase in the value of R4, which would offer difficulty in going to a hybrid IC version of the rebalance loop. Also, with the use of two amplifiers, it is quite simple to vary the dc gain by adjusting R7, without affecting the locations of the poles or zero.

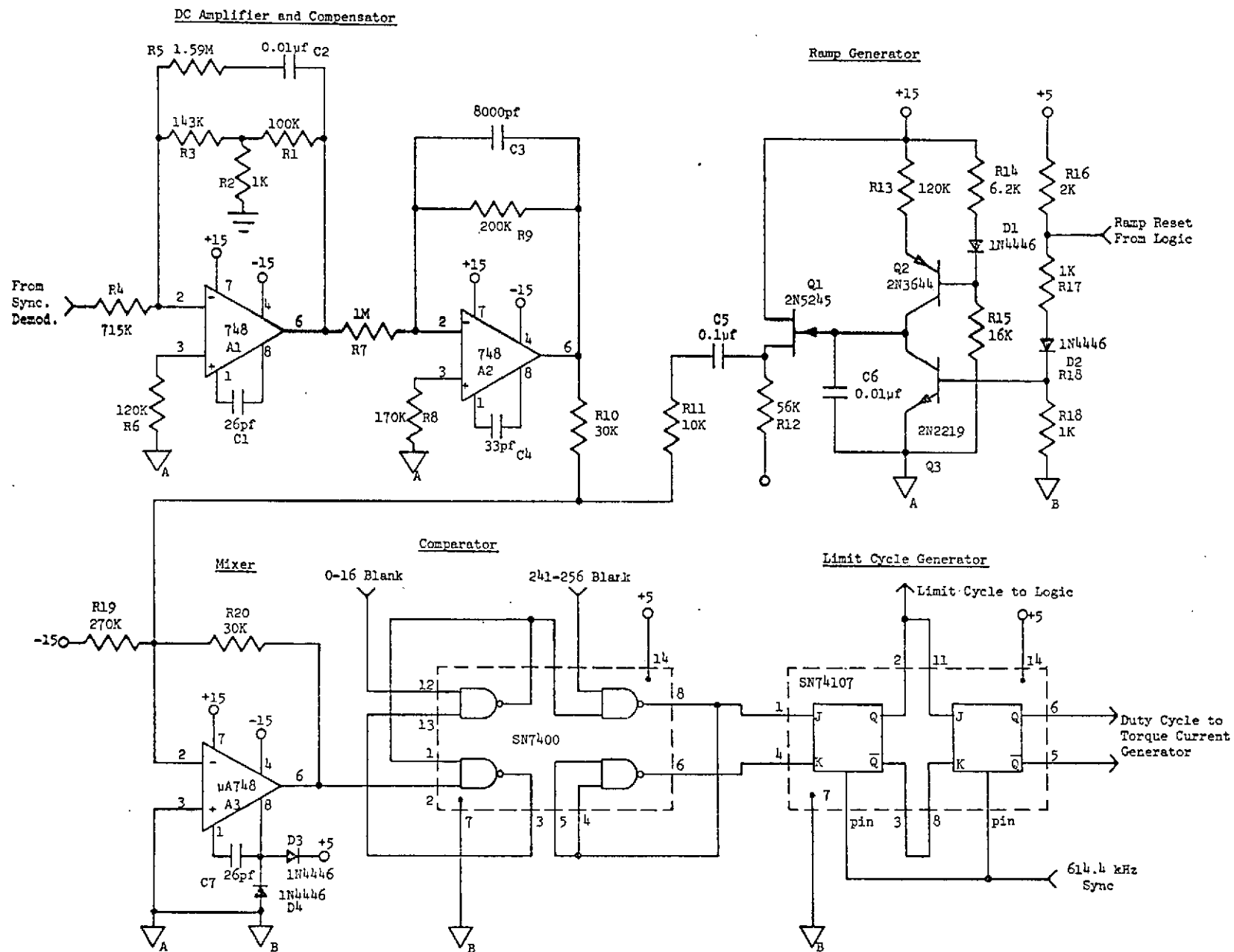


Fig. 5. DC Amplifier, Compensator, and Duty Cycle Generator.

From Eqs. (26) and (27) the overall dc gain is

$$\frac{V_{o2}}{V_{i1}} = \left(\frac{R3}{R4} \right) \left(\frac{R1 + R2}{R2} \right) \left(\frac{R9}{R7} \right) , \quad (28)$$

or substituting values

$$\frac{V_{o2}}{V_{i1}} = 4.04 . \quad (29)$$

Since the gain (dc output/ac peak input) of the synchronous demodulator was chosen as unity, Eq. (29) is also the gain from the input to the synchronous demodulator to the input to the comparator section.

From Eqs. (26) and (27) the pole locations are

$$\omega_{p1} = \frac{1}{C2[R5 + R3(1 + R1/R2)]} , \quad (30)$$

and

$$\omega_{p2} = \frac{1}{R9 C3} , \quad (31)$$

while the zero location is

$$\omega_z = \frac{1}{R5 C2} . \quad (32)$$

Substituting circuit values gives $f_{p1} = 1\text{Hz}$, $f_{p2} = 100\text{Hz}$, and $f_z = 10\text{Hz}$, which are the required values obtained earlier for compensation of the re-balance loop.

The resistors $R6$ and $R8$ are included to reduce the dc drift due to

input base current offsets for A1 and A2.

Duty Cycle Generator

The duty cycle generator (Fig. 5) is similar to the Hamilton Standard design discussed in references 1 and 2. The ramp signal and the processed error signal are mixed at the input of amplifier A3. The output of A3 is a positive error signal which is run down by the negative slope ramp. When the composite signal crosses the threshold (about +1.3 volts) of the SN7400 comparator gate (Fig. 5), the output J-K flip-flop changes state and thus proportions the torque current between positive and negative values. Voltage clamps in the mixer A3 limit the input signal to the comparator to TTL operating levels. The mixing resistors at the op amp input can be changed to vary both the ramp slope and the error signal slope. Of course, this is just a simple gain change.

The blanking signal inputs to the duty cycle generator from the logic set lower bounds to the duration of positive and negative torque currents. The limit-cycle signal to the logic carries the torquing rate information.

The duty-cycle generator logic functions are performed by TTL logic to be compatible with the Hamilton Standard TTL logic that is now being used with our rebalance loop. The new CMOS logic block now under development will necessitate a change to CMOS logic functions in the duty cycle generator.

Torque Current Generator

A reliable and accurate strapdown sensor system requires that the rebalancing torquer be driven by very accurate current pulses with well-defined amplitude, duration, and shape. The requirement of a precisely known weight for each torque pulse strongly constrains the design of the

torque current generator in the pulse rebalance electronics.

The torque current generator performs a two-fold function. First, it regulates the magnitude of the torque pulse current by referencing it to a precision voltage reference and a high stability sampling resistor. Second, it has the capability of torque scaling, i.e., changing the weighting of the torque pulses by changing the magnitude of the loop current.

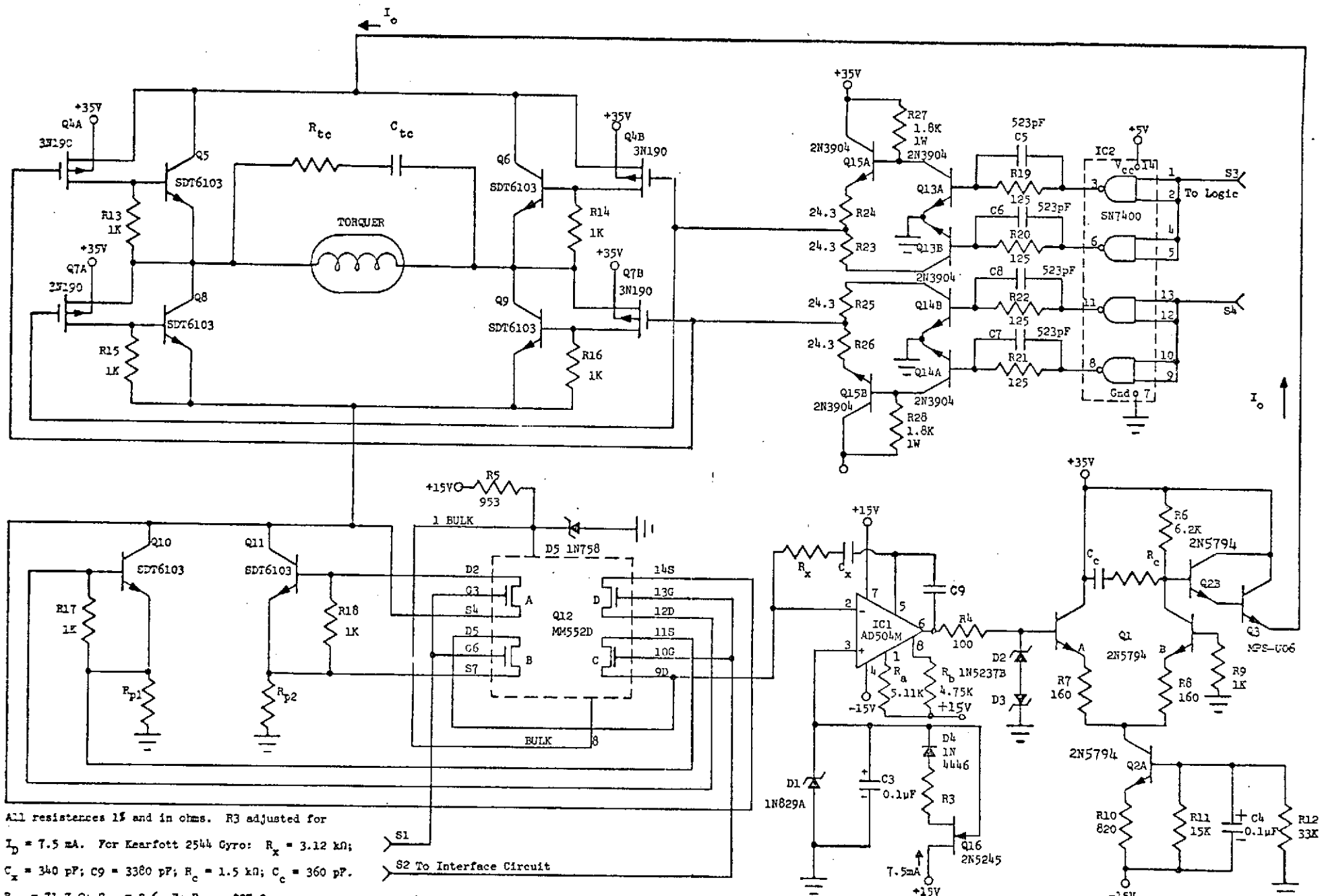
The torque current generator illustrated in Figure 6 is the to-date result of pursuing a goal at U.T. of designing a near optimum, yet versatile, torque current generator for use in a strapdown sensor system. An effort has been made to incorporate the best aspects of previously published torque current generators as well as the inclusion of improved solid state devices. The torque current generator consists of a dc feedback loop containing the following: a precision Zener diode driven by a constant current source and serving as a precision voltage reference; a comparator operational amplifier; an error amplifier serving as a level shifter; a power transistor which functions as the output stage of the current regulator; an H-switch; an H-switch driver; two precision sampling resistors with a sampling resistor switching network; a TTL to CMOS interfacing circuit; and torquer compensation. Each of these functional blocks will now be discussed.

The Precision Voltage Reference. The application here requires a precision voltage reference with ultra-high stability of voltage with time and temperature change. An MZ605, with its voltage time stability of $< 5\text{ppm}/1000\text{ hr.}$ and temperature stability of $5\text{ppm}/^{\circ}\text{C}$, could have been used for the precision reference diode. However, due to economics and resolution of available measuring instruments, a 1N829A was chosen as a reasonable substitute. This Zener reference diode has an average temperature coefficient,

over the operating temperature range, of $\pm 5\text{ppm}/^{\circ}\text{C}$. In addition, the diode has a low dynamic impedance and a silicon oxide passivated junction for long-term stability.

For additional stability in V_z , I_z is furnished by a JFET constant current source, Q16 (see Fig. 6). Resistor R3 and diode D4 properly bias Q16 to deliver 7.5mA, while D4 also improves temperature stability of Q16. Capacitor C_3 is a 0.1 μF capacitor which helps suppress noise produced by the Zener reference diode, and reduces coupling of high frequency power supply signals back into the loop.

The Comparator Operational Amplifier. Normally, the objective in selecting the amplifier IC1 of Fig. 6 would be to choose the least expensive device which would meet the physical, electrical, and environmental requirements imposed by the application. This would suggest a "general purpose" amplifier. However, accuracy and stability constraints for the case at hand require the lowest offset and drift parameters possible. Also, a very high common-mode rejection ratio (CMRR) is useful. A large open-loop gain is demanded to provide a sufficiently high loop transmission, which in turn will give the required degree of accuracy. Accuracy, along with offset and drift parameter requirements, overshadow gain-bandwidth considerations in selecting the amplifier. However, an amplifier which will assure an adequate value of loop gain at the maximum frequency of interest is necessary for the desired accuracy. It is necessary that the input of the amplifier be protected, since in Fig. 6 it is required to switch from a 41.3 Ω sampling resistor to a 207 Ω sampling resistor, in approximately 350 nano-seconds. To limit over- and under-shoot in the pulse response and to maintain close regulation, it is essential that the amplifier have as large



NOT REPRODUCIBLE

Fig. 6. Torque Current Generator

a slew-rate capability as possible.

The above mentioned criteria, along with items of lesser interest, were studied closely. After detailed investigations and testing, it was found that the Analog Devices AD504M offered the best overall performance. There appears to be a fundamental limitation in achieving both a very high loop gain with stability and a suitable slew-rate. This has been partially alleviated by the use of a feedforward technique (R_x and C_x in Fig. 6). The feedforward technique makes it possible to more heavily compensate for stability with C_9 and the RC lag network (R_c and C_c), and yet obtain a reasonable slew-rate with IC1. While the transient response was acceptable for a 2 to 1 scale factor change, more work is needed to provide better slewing rate, overload recovery, and settling time for a 5 to 1 scale factor change.

If the AD504 amplifier is to exhibit its superior drift performance, the manufacturer recommends that the device be nulled. R_a and R_b in Fig. 6 are typical values found from investigating three AD504M units.

The Error Amplifier - Level Shift Network. Q1(A and B) in Fig. 6 is a differential pair following the input IC1 comparator and functions in a dual role as an error amplifier and level shifter. Q2A serves as a constant current source to supply Q1. D2 and D3 (1N5237B with $V_z = 8.2V$) serve to clamp the signal excursions at the base of Q1A and prevent saturation of either Q1A or Q2A; the diodes are normally not conducting. Resistors R7 and R8 in the emitters of Q1A and Q1B increase thermal stability and decrease the gain of this stage. The RC lag network (R_c and C_c) across the collectors of Q1A and Q1B helps shape the frequency response of the torque current generator.

The error amplifier is operated in the noninverting mode to reduce any Miller effect at the base of Q1A and hence improve the frequency response. While duals (2N5794) were used for Q1 and Q2, a quad NPN such as the MHQ2222, or individual 2N2222 transistors would serve as well.

The Power Transistor Stage. A Darlington configuration is used for the output stage of the current regulator. One half of a 2N5794 drives the medium power transistor, Q3. An SDT6103 may be used for Q3, but tends to operate at an elevated temperature. An MPS-U06 was a better choice, and operates much cooler when properly heat-sinked. The Darlington configuration used here does not load the collector circuit of Q1B, and has a current drive capability that far exceeds the required 150 mA.

The H-Switch. The H-switch is a modification of the H-switch in the Hamilton Standard system outlined in the Lawrence Report.² The H-switch is a bridge arrangement consisting of four composite MOSFET-bipolar transistor switches. All the MOSFETs in the H-switch of the U.T. system are P-channel, whereas in the Hamilton Standard version two P-channel and two N-channel MOSFETs were used. Since dual N-channel MOSFETs are at present unavailable commercially, matching was more easily accomplished with P-channel devices. A dual P-channel MOSFET with separate source and drain leads is necessary in the lower switches of the H-switch, i.e., for Q7A and Q7B in Figure 6. The type 3N190 P-channel MOSFET was used for both Q4 and Q7 in the H-switch. It has a maximum $r_{DC(on)}$ of 300Ω , 10% matching of Y_{fs} , and is readily available from several manufacturers. Also, it has a minimum BV_{DSS} of 40V, which is difficult to obtain in many of the other available dual MOSFETs.

Each composite switch in the H-switch contains a bipolar transistor as well as a MOSFET. Type SDF6103 bipolar transistors were chosen to fill this role. This device has a BV_{CEO} of 50V, a maximum collector current rating of 5 amperes, and a total power dissipation (with a TO-5 case) of 7W. It has a maximum turn-on and turn-off time of 50 nanoseconds, an f_T of approximately 450 MHz in the region of interest, and a beta curve which is almost flat in the region of interest.

The H-switch, composed of the four composite MOSFET-bipolar switches discussed above, has excellent electrical isolation from the H-switch driver circuit. This was discussed in the U.T. Annual Report¹ of 1972. The composite MOSFET - bipolar switches have excellent thermal stability, as pointed out in the Masters Thesis given as Reference 4.

The H-switch Driver. This circuit has the function of translating a state in the logic section into a torque current polarity. When instructed by the logic, it sets up the H-switch to route the torquer current in the necessary direction through the torquer to null the error signal.

The H-switch driver is designed to relegate any limitations in switching speed to the H-switch itself. Since the H-switch driver is essentially driving a capacitive load, considerable effort was necessary to acquire suitable switching times for the 0-35V excursions. Best results were obtained using bipolar transistors with active pull-ups and active pull-downs in the output stage of the driver circuit. In Figure 6, Q15A and Q15B are the output stages; Q13A and Q14A function as active pull-downs, rapidly sweeping base charge out of the output stage turning off; Q13B and Q14B serve as active pull-ups to rapidly charge the output capacitance of the output stage turning off. The RC networks connecting the SN7400 IC to

Q13 and Q14 are commutating networks. The SN7400 serves as the input section of the H-switch driver circuit.

The H-switch driver circuit also serves as an interfacing circuit for TTL to MOSFET levels. When the CMOS logic is ready, a modified version of this H-switch driver will be substituted. The modified version has already been experimentally checked, and will be detailed in a doctoral dissertation to be published at a later date. Switching times on the order of 20 nanoseconds have been obtained with both versions of the driver circuit.

The Sampling Resistors and Sampling Resistor Switching Network. Two sampling resistors are required in this design since the precision voltage reference (PVR) is held constant. With the PVR chosen at 6.2V, values of R_{p1} and R_{p2} were then chosen to give desired current levels and scale factor ratio. For current levels of 30 mA and 150 mA, or a scale factor ratio of 5 to 1, R_{p1} and R_{p2} are required to be approximately 206.7 Ω and 41.3 Ω , respectively. To date, the torque current generator has been operated with 30 and 150 mA levels, and also with 30 and 60 mA levels. The 60 mA high requires R_{p2} to be approximately 103.3 Ω . The wattage of the sampling resistors should be 3W minimum. Naturally, the sampling resistors need to be as stable as economics and availability allow, and if wirewound, should be as noninductive as possible.

The sampling resistor switching network consists of a quad MOS analog switch (MM552D, a four MOS transistor package), two type SDT6103 bipolar transistors, and resistors R17 and R18. Transistors Q10 and Q11 are paired with Q12D and Q12A respectively to form two composite MOSFET - bipolar switches. Q12B and Q12C serve as buffer switches between the sampling

resistors and the comparator amplifier.

The quad MOSFET analog switch is biased at approximately 10V to ensure that the inherent diodes formed from source and drain to the substrate are never forward biased. This is also required because the voltage at the base of the H-switch (emitters of Q8 and Q9) may be as high as 8 volts. The 10V bulk bias is obtained from the 15V supply by means of R5 and D5, which eliminates the need of a separate 10V supply. Biasing the quad MOS analog switch at 10V requires a gating voltage of approximately zero to 10V. If the switch is driven by CMOS logic, this is no problem. However, if the switch is driven by TTL logic (as is the case until the new CMOS logic can be constructed and experimentally evaluated), then interfacing is necessary. A circuit which will perform this interfacing function satisfactorily is given in Figure 7 and is discussed next.

The Interfacing Network. The TTL to CMOS interface circuit mentioned immediately above (and shown in Fig. 7) is identical to the H-switch driver circuit, except for having a 10V supply instead of a 35V supply. The 10V supply is obtained from the 15V supply by means of Q23 and associated resistors. This circuit is given in Figure 7, along with the TTL to CMOS interface circuit. Under actual load conditions, the 0-9.6V excursions at the output of the interface circuit are approximately 60 nanoseconds and 16 nanoseconds respectively for the 10-90% rise and fall times. The interfacing circuitry in Figure 7 is unnecessary if CMOS logic is used.

Torquer Compensation. The torquer compensation network depends of course upon which gyro is being used. The goal is to make the torquer coil look purely resistive. For the Kearfott Model 2544 gyro, experimental measurements indicate a torquer inductance of 3.08mH, a torquer resistance of

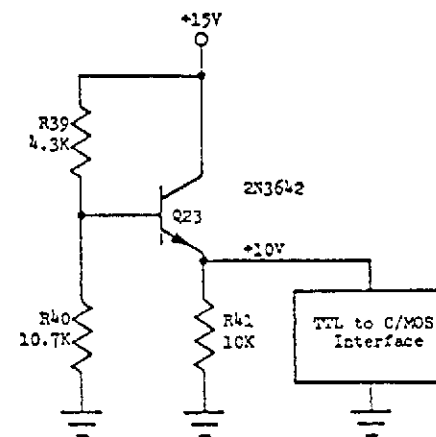
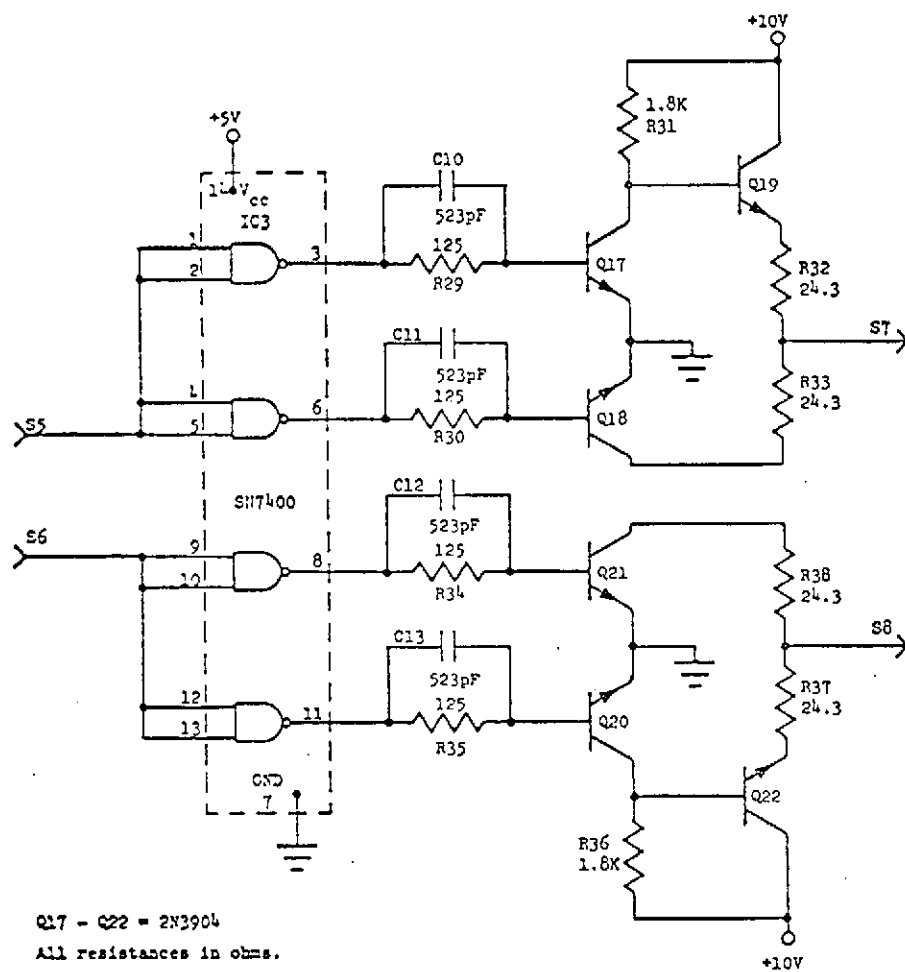


Fig. 7. TTL to C/MOS Interface.

71.7 Ω , and a stray capacitance of 20.4 pF. Consequently, to compensate the torquer of this gyro, R_{tc} and C_{tc} in Figure 6 need to be 71.7 Ω and 0.60 μ F, respectively. The strap capacitance was not compensated.

The preceeding few pages have been utilized to discuss the basic design and function of each of the major divisions of the torque current generator. A brief discussion of some of the salient features of the design will now be given.

Versatility of the Torque Current Generator. The torque current generator, as it is shown in Fig. 6 is designed to receive commands from TTL logic. However, by modifying the H-switch driver circuit, and eliminating the TTL to CMOS interfacing circuit driving the sampling resistor switching network, the torque current generator is ready to receive commands from CMOS logic. Naturally, the power consumption would drop considerably.

The range of torquing current available from the torque current generator depends heavily upon the gyro torquer being driven. For the Kearfott Model 2544 gyro, preliminary calculations indicate that the torque current generator can deliver torquing current in a range of 1 mA to 275 mA and still maintain tight control. Of course the Kearfott Model 2544 is not designed to handle that magnitude of current, but its torquer resistance was used to obtain the above range. The indications are that even lower currents are possible (as well as higher), and more on this subject will appear later in a doctoral dissertation.

Reduction of the Number of Power Supplies. Initial studies indicate that there is a real possibility of eliminating the 35V supply if high torque currents are not required. In that case, the torque current generator

would need +15V, -15V, +10V, and a +5V supplies. Furthermore, when the CMOS logic replaces the TTL logic, the 5V supply can be eliminated. The 10V supply can easily be obtained from the 15V supply. The torque current generator would then require only +15V and -15V supplies.

There is insufficient data on the manufacturer's data sheet for the SDT6103 to accurately calculate offset static and drift errors in the current sensed by the sampling resistors. However, if one assumes a probable maximum $I_c(\text{off})$ to be 20 nA for the SDT6103, then an estimate can be made. This assumption, together with data on the 3N190 and the equations developed in Reference 1, yields a static error of ≤ 0.56 ppm if $I(\text{low})$ is 71.5 mA. If $I(\text{low})$ is 30 mA, the torque static error is ≤ 1.4 ppm. The drift error is likewise estimated to be ≤ 0.06 ppm/ $^{\circ}\text{C}$.

The torque current generator has been experimentally tested using both the Honeywell GG334 and Kearfott 2544 gyros. It has performed as anticipated in both cases.

With the Kearfott Model 2544 gyro, the torquer current was switched from one sampling resistor to the other in approximately 350 nanoseconds. The complete settling time required approximately 15 μsec . The H-switch driver circuit's output has a 10-90% risetime of 20 nanoseconds, and a 90-10% fall time of 10 nanoseconds. The TTL to CMOS interface circuit has 10-90% rise and fall times of 60 nanoseconds and 16 nanoseconds, respectively.

Logic

The logic now being used with our rebalance loop is the Hamilton Standard TTL logic discussed in reference 1. Our rebalance loop was designed for use primarily with +10 V CMOS logic but is sufficiently versatile to be used with the +5 V logic. The +5 V logic requires some interfacing networks

not needed for the +10 volt logic. For a detailed description of the operation of the TTL logic of Fig. 3, the reader is referred to reference 1.

A new CMOS +10 V logic is now under development. The current requirement will probably be no more than 10 mA (the TTL logic requires about 500 mA). Its input and output signals are the same as those of the logic of Fig. 3; however, the design philosophy is quite different.

CMOS Crystal-Controlled Clock

A timing circuit generally consists of three basic parts: an oscillator or main timing standard, some digital processing logic, and logic-circuit drivers for the electrical output devices. The logic circuit drivers are controlled by the digital processing logic. The oscillator, or clock, is possibly the most important because the accuracy of the total timing system is entirely dependent upon the accuracy of the oscillator.

A basic oscillator circuit consists of an amplifier and a feedback section. For oscillation to occur, the loop gain of the circuit must be greater than unity. In addition, the total phase shift through the amplifier and the feedback network must be $n360$ degrees, where n is an integer. The frequency stability of an oscillator depends primarily upon the phase-changing properties of the feedback network. For high stability, it is usually necessary to use a quartz crystal as a feedback element.

The oscillator circuit shown in Figure 8, is a typical CMOS crystal-oscillator circuit using a crystal pi-type feedback network. This type of feedback network is used because it is suitable for use with a parallel-resonant oscillator circuit. A parallel-resonant circuit works best with amplifiers that have high input impedances, and is thus most applicable to

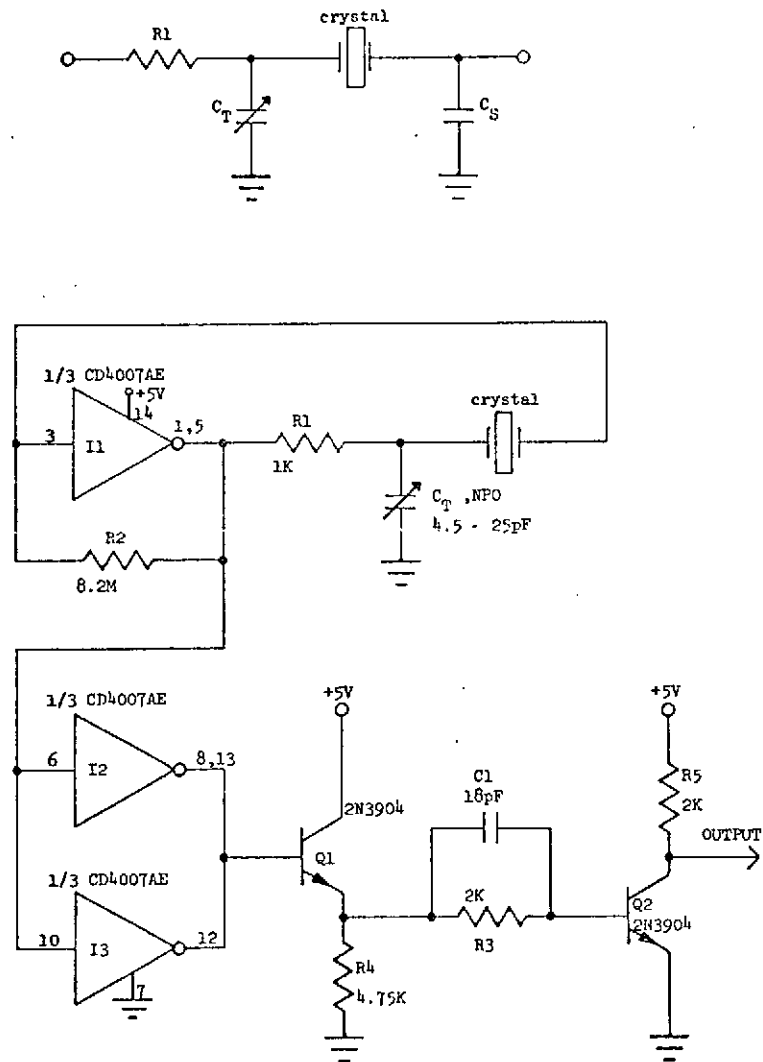


Figure 8. CMOS Crystal Controlled Clock.

crystal oscillators that employ CMOS amplifiers. In Fig. 8(a), C_{π} of the crystal pi-type feedback network is an NPO 4.5-25 pF variable capacitor. C_S is replaced by the input capacitance of the CMOS inverter, which is typically 5 pF. R_1 was experimentally chosen to be 1K. The crystal has a nominal value of 2.4576 MHz at its parallel-resonant frequency. Since a crystal of this precise frequency was not immediately available, a crystal with a nominal parallel-resonant frequency of 2.466 MHz was used in the implementation of the circuit at U.T. The 2.4576 MHz frequency is needed to provide the 614.4 kHz sync frequency and the 19.2 kHz pick-off frequency for the Kearfott Model 2544 gyro. Use of the 2.466 MHz frequency gives approximately a 3418 ppm nominal error in these two frequencies. The measured value of oscillation frequency was 2.466752 MHz plus or minus one digit. The measured values of the sync and pick-off frequencies used in the U.T. system were 616.688 kHz and 19.271 kHz, respectively.

The amplifier function is performed by I1 in Fig. 8, which is a CMOS dual complementary pair connected as an inverter. Resistor R_2 is a biasing resistor that enables the I1 logic block to function as a linear amplifier. This resistor should have a value high enough to prevent loading of the feedback network, but low in comparison to the amplifier input resistance. Resistor values from 8 M and 500 M are suitable. However, to allow greater input leakage without any major change in the bias point, a value in the lower section of this range is desirable. A value of 8.2 M was used in the experimental circuit at U.T.

The current consumption of the oscillator amplifier is strongly dependent upon the attenuation across the feedback network. As the attenuation becomes greater, the amplifier input signal becomes smaller, and this in

turn increases the amplifier current consumption. A feedback network with small attenuation is best in terms of power consumption.

The oscillator output is taken at the output of I1. If CMOS logic were being used, this output would be connected directly to the digital processing logic. However, at present the Hamilton Standard TTL logic is being used and interfacing was necessary. While a 5 V supply is allowable with CMOS as with TTL logic, the current-sinking and -sourcing capabilities of the CMOS oscillator are not sufficient to drive TTL logic. Two CMOS inverters (I2 and I3) are connected in parallel to the output of the oscillator. (I1, I2, and I3 are all contained on one CMOS chip, the CD4007AE). The parallel combination of I2 and I3 give an output drive of approximately 2 mA. The ability to sink 1.6 mA without the output rising above 0.8 volts was still lacking. Transistors Q1 and Q2 with their associated circuitry solved this problem. The output to the digital processing logic is taken at the collector of Q2 and has both the necessary current-sinking and -sourcing capabilities to drive TTL logic gates.

Power consumption of the CMOS oscillator is approximately 2 mW at a V_{DD} of 5 volts and a frequency of 2466 kHz. The oscillator current is approximately 0.4 mA. Addition of the interface circuitry necessary to drive TTL raises the power consumption to a conservative estimate of 800 mW.

The maximum frequency for which CMOS may be used depends heavily upon the power supply voltage used. For a V_{CC} of 5 volts, a frequency of 5 MHz or more is attainable. The experimental clock circuit of Fig. 8 was run at 5.8 MHz. It performed well at this frequency, although the waveforms were somewhat degraded when compared to those at 2.466 MHz.

Pickoff-Excitation Signal Generator

The signal generator, indicated in Fig. 9, supplies an 8 V rms sinusoidal signal for the Kearfott 2544 pickoff excitation, and also is coupled to the synchronous demodulator which is between the AC and DC amplifiers in the rebalance loop. The input to the signal generator is a 19.2 kHz signal from TTL logic that is synchronized in the logic section to the 2.4576 MHz clock. Since the TTL output can be in the range from 2.4 V to 4 V in its high state, and 0 to 0.8 V in its low state, the signal generator block must provide an initial fixed amplitude limiting, and then a conversion from a square-wave to a sinusoidal signal.

The fixed amplitude limiting function is accomplished in Fig. 9 by the A1 amplifier. The noninverting input of A1 (pin 3) is raised to +1.2 V, hence as the input TTL signal (on pin 2) increases above this value, the output of A1 will go to the lower limit of -0.5 V, set by the diode D1. When the TTL logic signal is in its low-state of -0.8V to 0 V, then the A1 output is at a positive voltage of $+15\text{ V} - V_{CE}$, or approximately +14 V. Thus the amplifier A1 is connected as a voltage comparator with fixed output levels. The 100 pf capacitor C3 (between pins 1 and 2) is connected in a feedforward arrangement, thereby improving the slew-rate of the 748 amplifier. One could improve the output amplitude stability by limiting the positive output drive with a Zener diode connected to pin 8 of A1. Unfortunately, however, most Zener diodes have a large capacitance, which degrades the pulse response of the amplifier.

The square-wave is converted to a sinusoid in an active filter network, comprising R1, R2, R3, C1, C2, the amplifier A2, and the output transistors Q1 and Q2. The Q of the filter was chosen as 4.5, thereby offering good

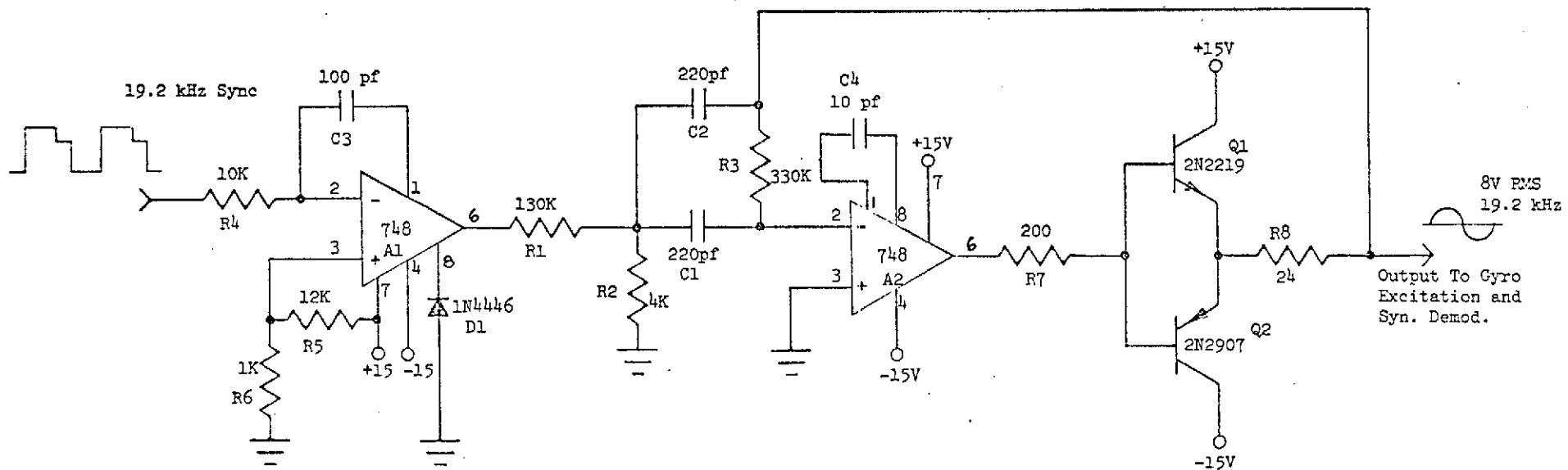


Fig. 9. Synchronous 19.2 kHz Signal Generator.

square-wave to sinusoid conversion, and yet still being sufficiently low to allow for center frequency offsets due to component tolerances. In this circuit, the center frequency can be shifted slightly by adjusting R2, while the output amplitude can be adjusted by changing R1. These adjustments are reasonably independent, since $R1 \gg R2$.

Since the Kearfott 2544 gyro requires a maximum of 30 mA drive current, which surpasses the limits of a 748 amplifier, a power driver circuit was included. This circuit is the Class B complementary emitter-follower 2N2219 and 2N2907 transistors (Q1 and Q2) of Fig. 9. As this stage is included within the overall feedback loop of the active filter, their cross-over distortion is minimized.

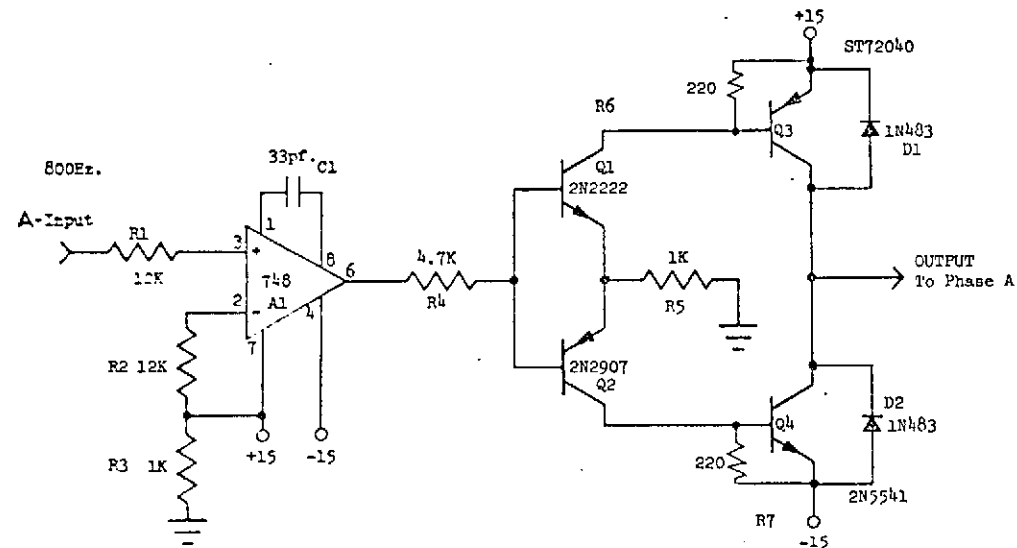
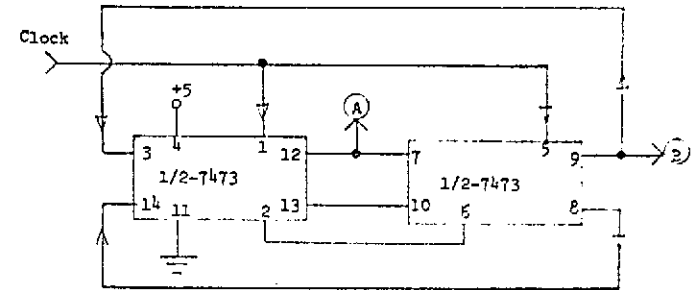
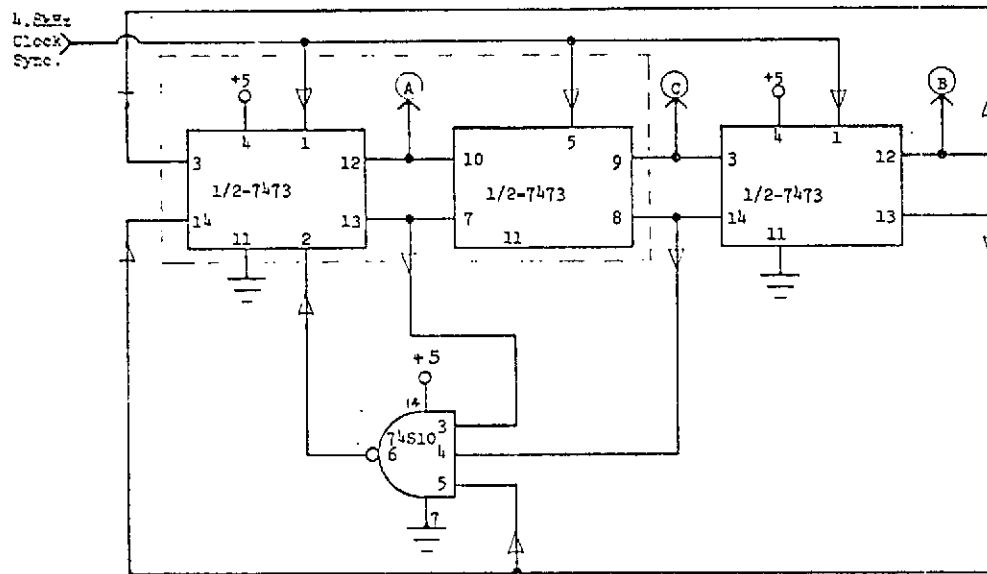
One could include more involved circuits to stabilize the output amplitude of the sine-wave, such as an AGC loop. However, since an amplitude change merely appears as an open-loop gain change in the overall rebalance loop, this added complexity was not deemed desirable.

Spin Motor Power Supply

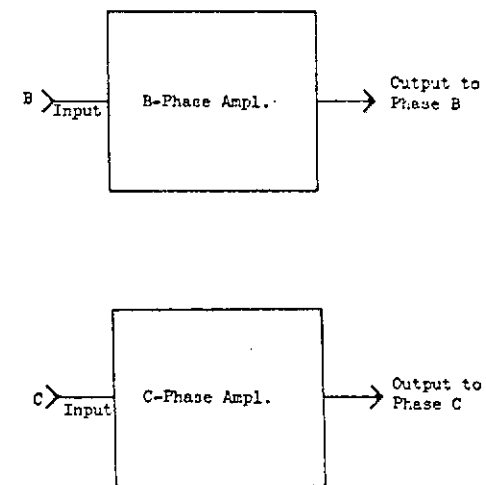
The Kearfott 2544 gyro requires a 26 V, 3-phase, 800 Hz power supply to drive the spin motor. A usual technique would be to use a 3-phase transformer to furnish power, however for system miniaturization this technique is not very compatible. A digital technique can be implemented as shown in Fig. 10. The circuit of Figure 10 was designed and built by E. H. Berry and Harry Reid of NASA-MSFC, Huntsville.

In Fig. 10 a 4.8 kHz clock signal, synchronized by a digital count-down circuit in the Logic Section to the 2.4576 MHz crystal, is the clock drive signal to three serially connected J-K flip-flops (SN7473). The

-Two Phase-



A-Phase Amplifier



B- and C-Phase Amplifiers, Identical to
A-Phase.

Fig. 10. Three-Phase Spin Motor Power Supply for Kearfott 2544 Gyro.

output of the last flip-flop is connected to the J-K inputs of the first, and the 74S10 Nand gate is utilized as a gating signal at startup to ensure the correct phase sequence between the three phases. In this way the output of each J-K flip-flop section is the clock frequency divided by six, with a total of three outputs available that effectively splits the clock frequency of 4800 Hz into $4800 \div 6$ or three 800 Hz segments, equally spaced in time. Thus, one has available three 800 Hz frequencies, each exactly spaced by a phase difference of $360^\circ/3$, or 120° apart.

The output drive of Fig. 10 is a square-wave signal driving between saturation limits of ± 13 to 14 volts. Although the transients on the power and ground lines are increased by the use of a square-wave drive signal, the power dissipation in the output power transistors Q3 and Q4 is considerably reduced over a sinusoid output signal.

The Honeywell GG334 gyro requires a 800 Hz, 36 volt, two-phase-with-neutral power supply. This can be obtained by utilizing two J-K flip-flops, so that the input clock signal is divided by four. The two-phase block is also shown in Fig. 10. The square-wave power-driver circuit is the same as that for the Kearfott 2544 gyro, except that the power supply for the four output transistors (Q1 - Q4) for each phase is increased to the required value of 32 to 36 volts. The amplifier A1 must still operate on ± 15 V supplies.

EXPERIMENTAL RESULTS

The rebalance electronics loop was constructed and evaluated using both the Honeywell GG334 and Kearfott 2544 gyros. Previous to connecting the gyro's, the operation of the electronic system from the AD520 preamplifier input to the comparator output (see Fig. 3) was evaluated in terms of gain and phase-shift, and correct system operation was verified. The H-switch and current regulator loop had been previously verified. Then, with the gyro connected, the experimental data included evaluation of the loop transmission, the system transient response to an applied rate input, the effects of switching modes from low- to high-torque, the evaluation of uncertainties in the data transmission, and system resolution.

Since MSFC had expressed more interest in the 2544 gyro, most of the experimental data was obtained with this gyro in the loop.

The Honeywell GG334 Gyro

With the GG334 gyro initially connected and the electronics loop open, the float was driven to both limits to observe if the system would accept a worse-case overload. It was found that due to the excessive phase-shift produced by A4 (in Fig. 4) in saturation that it was possible for the output of the demodulator A5 (in Fig. 4) to change sign. Had this occurred in a closed-loop connection, it would have produced a positive feedback condition, with resultant latch-up. The active clamp circuit (Q1 - Q2, Fig. 4) in the A4 amplifier was introduced, which then allowed full motion of the float to either stop, without sign change at the demodulator output.

The filter section (A2, A3 of Fig. 4) was operated at a center frequency of 32 kHz (in Fig. 5 this required that $R1 = 30K$, $C = 100$ pf, $R2 = \infty$, and $R5 = 91K$), to agree with the GG33⁴ specifications, and the signal generator input was 5V rms at this frequency. Initially, the gain of the electronics section was approximately a factor of two higher than the design goal, however it was found that the loop gain could be increased by 20 db above the design value and still maintain closed-loop stability. The loop transmission was experimentally checked from -20 db below the cross-over frequency (f_{cl} of Fig. 2) to +50 db above f_{cl} , and the results agreed with the expected theory. The loop gain was decreased by a factor of 100,000 (-100 db), and the system would still lock-in to null the gyro.

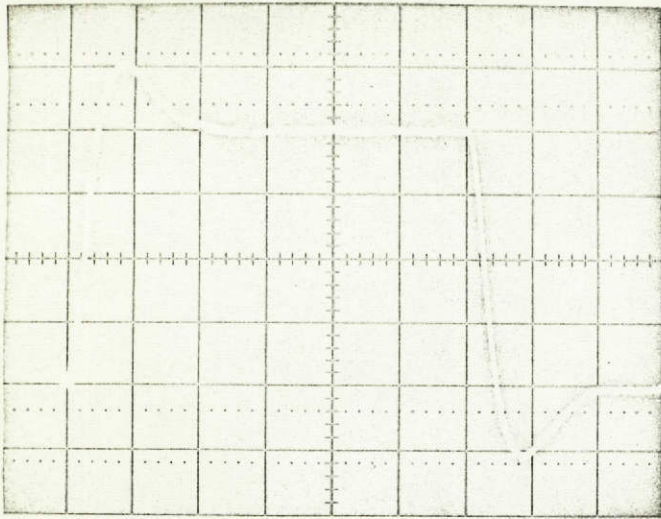
With the system operating in the normal configuration with low torque (30 mA) required, the output data uncertainty was evaluated, using a frequency counter. With normal loop gain the short-term (230 sec) min-max deviation in output count was 38 ppm. A decrease of loop gain by 80 db produced a deviation of 160 ppm, while with 100 db gain reduction the deviation was 680 ppm. This data was taken under lab conditions ($T \sim 25^{\circ}C$), with the spin motor not connected, but with full heater control applied to the gyro. The clock input was 4.0955 MHz.

The system was then checked with full spin motor power applied. Even though the spin motor supply was not synchronized to the logic clock, the data resolution observed was approximately ± 2 data pulse, or from Eq. (20), a resolution $\sim \pm 0.24$ arc-sec.

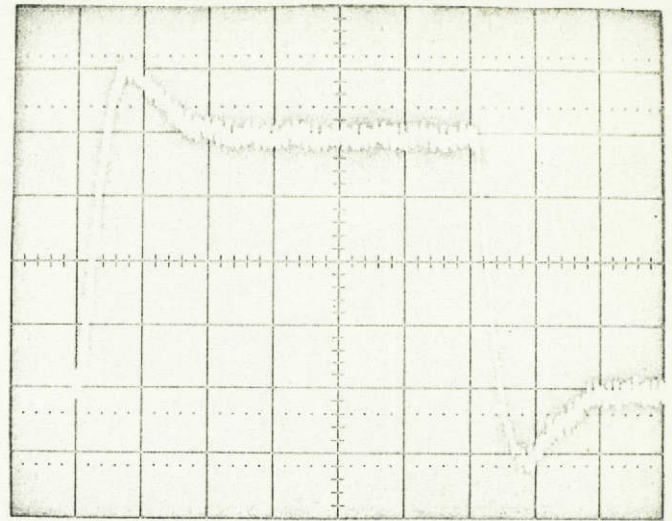
The Kearfott 2544 Gyro

The circuit diagram for the Kearfott 2544 gyro with the rebalance electronics was shown in Fig. 3. The system was tested with a clock crystal oscillator of 2.466752 (stability of ± 1 ppm), so that the synchronization frequencies were 616.688 kHz, 19.271 kHz, 4.818 kHz, and the spin motor power supply operated at 803 Hz. The signal generator and spin motor supply were synched to the logic as stated earlier. With the spin motor off, full temperature applied to the gyro, and gravity correction applied, the data uncertainty was estimated as within $1/4$ data pulse (0.05 arc-sec) and the spread in low-torque data counts was a min-max of 32 ppm for a short-term period of 100 sec. With the spin motor turned on, the resolution values were ± 1 data pulse (± 0.2 arc-sec) and 32.5 ppm.

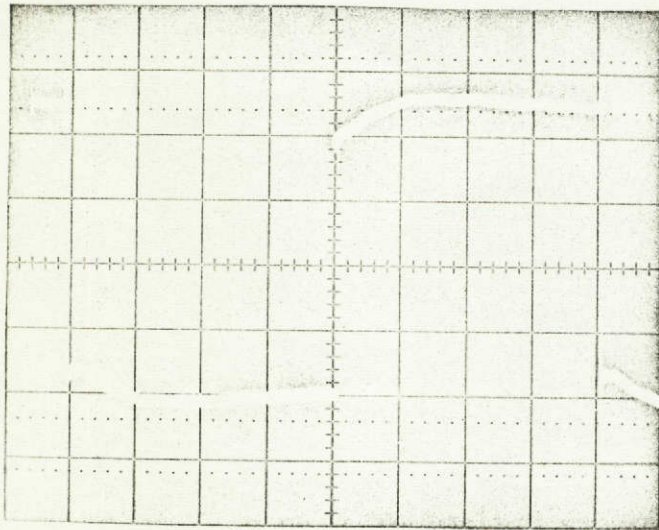
For the Kearfott 2544 system, the observed closed-loop response to a step function input is shown in Fig. 11a with the spin motor off, and in Fig. 11b with the spin motor on. The waveform of the voltage applied to the compensated torquer winding (for 30 mA torque current) is shown in Fig. 11c, and the waveform for the torquer current applied is indicated in Fig. 11d. The observed rise-time (10-90%) of the closed-loop response is about 7 msec, which is consistent with the design value of 40 Hz for f_{cl} . The observed rise- and fall-times for the current pulse through the torquer were 70 nsec and 90 nsec, respectively. In Fig. 12 is shown the transient response of the current through the torquer as the torque current is being switched from a low value of 30 mA to a high value of 60 mA. The pips are from the 19.2 kHz synchronous generator frequency. Although the rise and fall times (10-90%) are approximately 5-10 μ sec, the total settling time is 12 μ sec. Since a data period is 1.63 μ sec, this represents a total



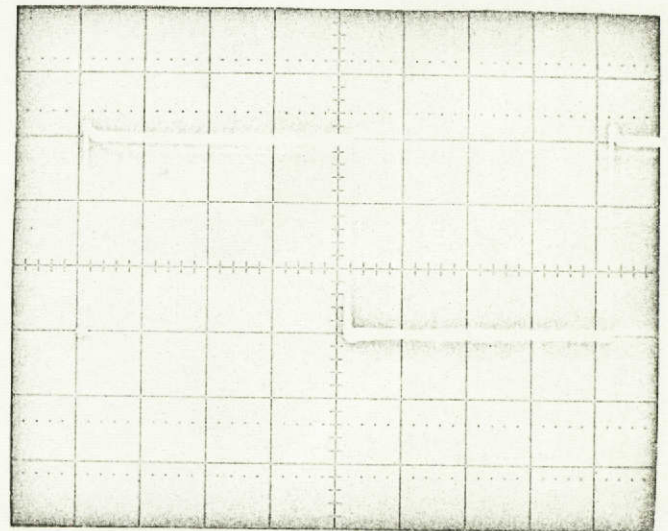
(a) Closed-loop response at comparator output, spin motor off; 0.1V/div., 20 ms/div



(b) Closed-loop response at comparator output, spin motor on; 0.1V/div, 20 ms/div.

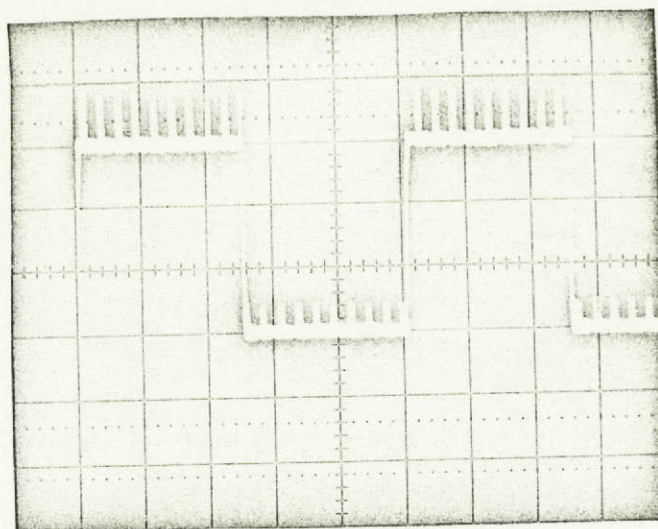


(c) Voltage across torquer, spin motor on, low torque (30 mA); 1V/div, 50 μ s/div.

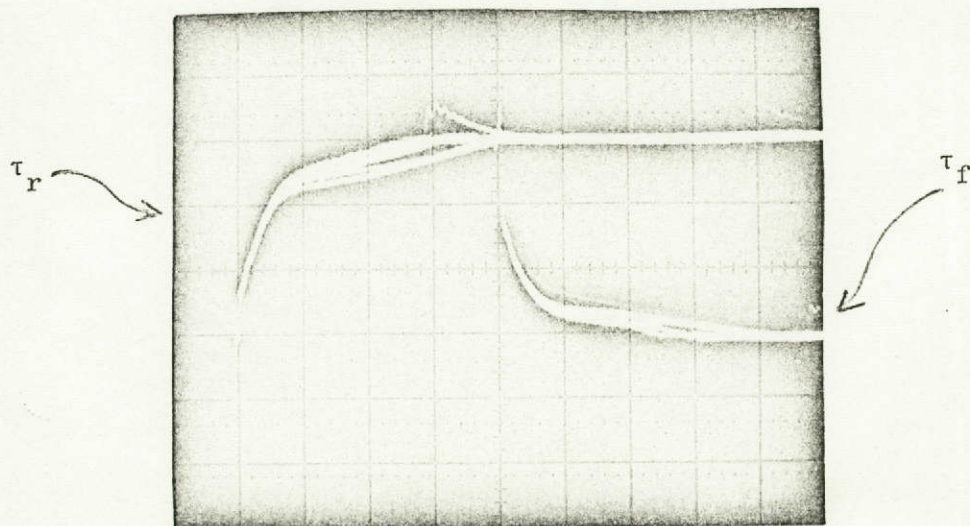


(d) Current through torquer, spin motor on, low torque (30 mA); 20 mA/div, 50 μ s/div.

Fig. 11. Transient Response Waveforms for the Kearfott 2544 gyro System.



(a) 10 mA/div, 500 μ s/div. Switching rate of 390 Hz.



(b) Rise- and fall-times of current; 10 mA/div, 5 μ s/div.

Fig. 12. Transient Response of Torquer Current When Switched from low- to -high scale (30 mA to 60 mA). Spin Motor On.

period of 8 data periods required to switch ranges. No attempt was made to "tune" the torquer compensation to lower the settling time.

The loop transmission for the Kearfott 25⁴⁴ system was checked experimentally over the range from 5 Hz to 80 Hz, and agreed with the theoretical design.

PROPOSED WORK

Several areas have been identified where additional work is needed to improve the rebalance electronics for strapdown gyroscopes. The areas will be briefly discussed in this section.

CMOS Logic Development

The new CMOS logic now being implemented should be completed and evaluated. The CMOS logic operation should be compared with that of the Hamilton Standard TTL System to determine which design philosophy is best for the width-modulated binary loop. If the Hamilton Standard logic is found to be superior, then it should be converted to a CMOS design.

Low Current Operation of the Torque Current Generator

The torque current generator was designed to be operated over a wide range of torque currents; however, it has not been carefully evaluated at currents below 30 mA. Since there are applications at currents as low as 1 mA, the generator should be operated, evaluated, and perhaps modified for the low current operation. The effects of switching transients and the degree of compensation of positive and negative torque current switching transitions should be evaluated at low currents.

Scale Factor Switching Speed

Although the scale factor switching speed is quite fast for our system (approximately the duration of 8 data pulses), it is desirable to switch the torque current in less than the period of one data pulse. Since our studies indicate that it may be feasible to accomplish the one data pulse switching speed, we believe that this goal is worthy of some additional effort.

Drift Effects in the Torque Current Generator

Further analytical and experimental studies of short and long term drift effects in the torque current generator is needed. These studies should be performed for the entire range of torque currents that the generator is capable of producing.

Reduction of Number of Supply Voltages

Attempts should be made to further reduce the number of required power supply voltages required for the rebalance loop. After incorporation of the CMOS logic, it will probably be feasible to operate the entire loop from only two supply voltages such as ± 15 volts for low torquing currents.

Higher Sample Rates

Efforts should be made to operate the rebalance loop at higher sample rates. This would allow higher data rates, larger closed loop bandwidths, and higher values for loop transmission. An increase of the sample rate to 10 kHz is probably feasible.

Loop Transmission Requirements

Some of the criteria for synthesis of the loop transmission were "rules-of-thumb". A thorough study of pickup noises, vibration modes generated, and other contaminating signals would perhaps yield information from which a more systematic design of the loop transmission could be accomplished.

Hybridization

The entire breadboard rebalance loop was designed so that it could be easily hybridized. The next step then is to realize the rebalance loop in hybrid form. This represents a rather significant change in layout and, thus, will require additional evaluation and perhaps some design adjustments.

References

1. Scientific Report S-23, "A Study of Strapdown Platform Technology", Chapter Five, NASA Contract No. NAS8-27296/DCN 1-1-40-10230, Dept. of Electrical Engineering, The University of Tennessee, Knoxville, Tennessee, 1972.
2. A. W. Lawrence, et. al., "The Design of an Advanced Strapdown Gyroscope," NASA Contract No. NAS12-687, Hamilton Standard System Center, Feb. 15, 1970.
3. Tobey, et. al., Operational Amplifiers, Burr-Brown Research Corporation, McGraw-Hill, pp. 291-293, 1971.
4. R. D. McKnight, "A Comparison of Two Current Regulator Loops for a Strapdown Gyroscope," M.S. Thesis, Dept. of Electrical Engineering, University of Tennessee, Knoxville, Tennessee, December, 1972.